FIG. 1

Prior Art

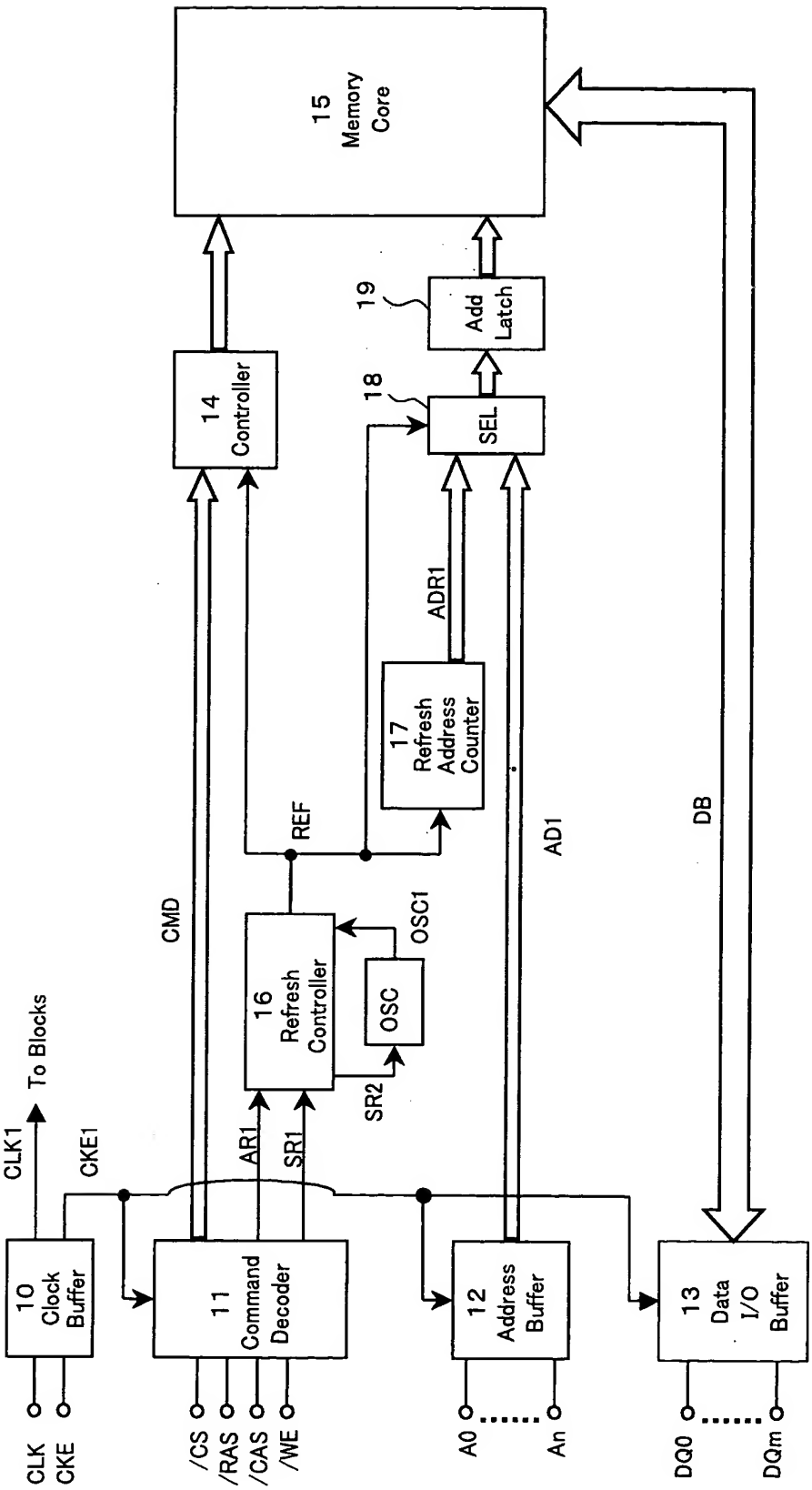


FIG. 2

First Embodiment

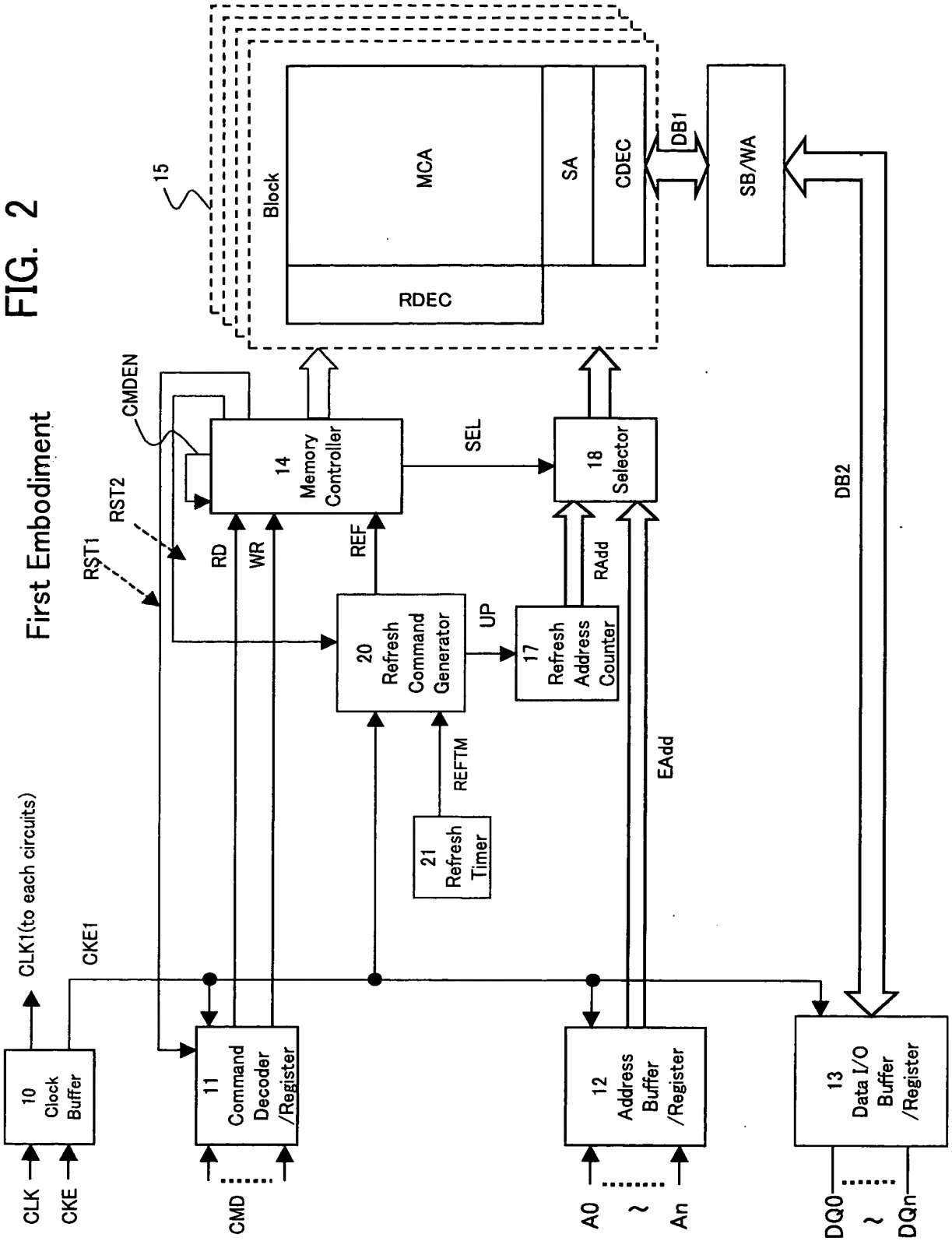


FIG. 3A

Clock-synchronous Operation

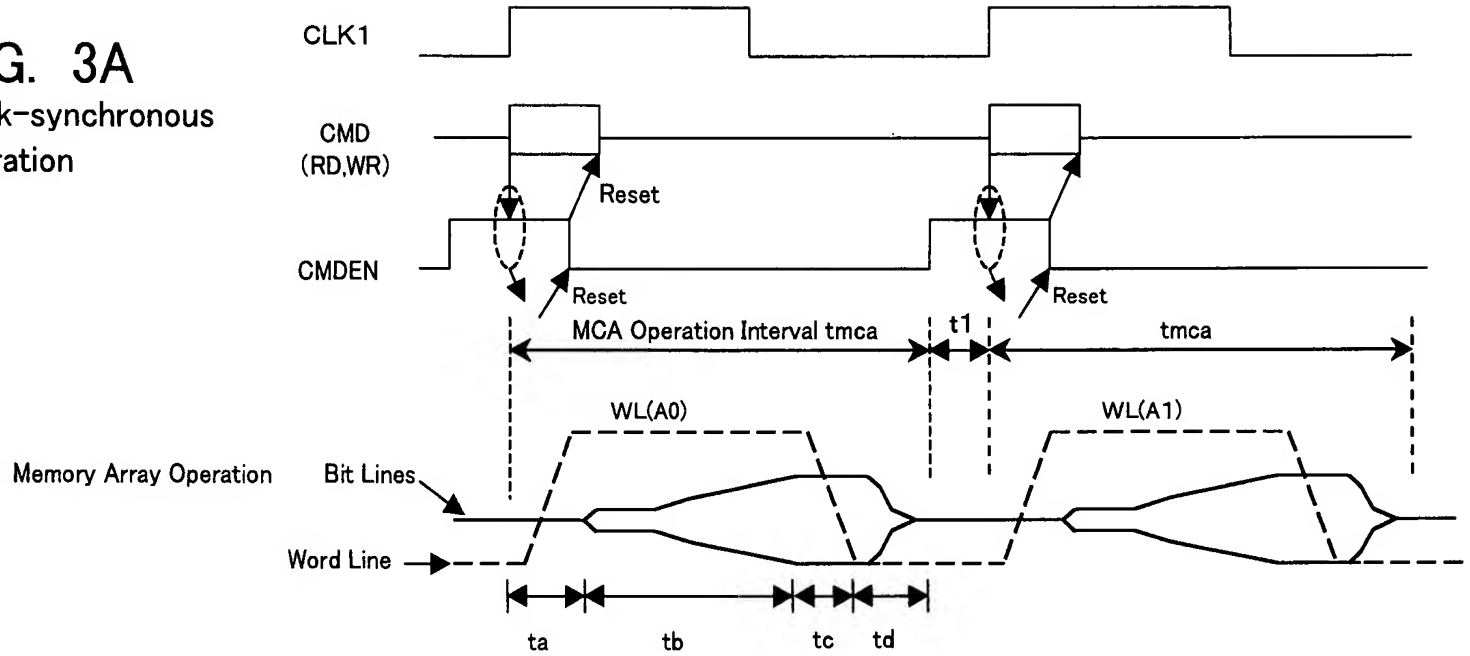


FIG. 3B

Clock-asynchronous Operation

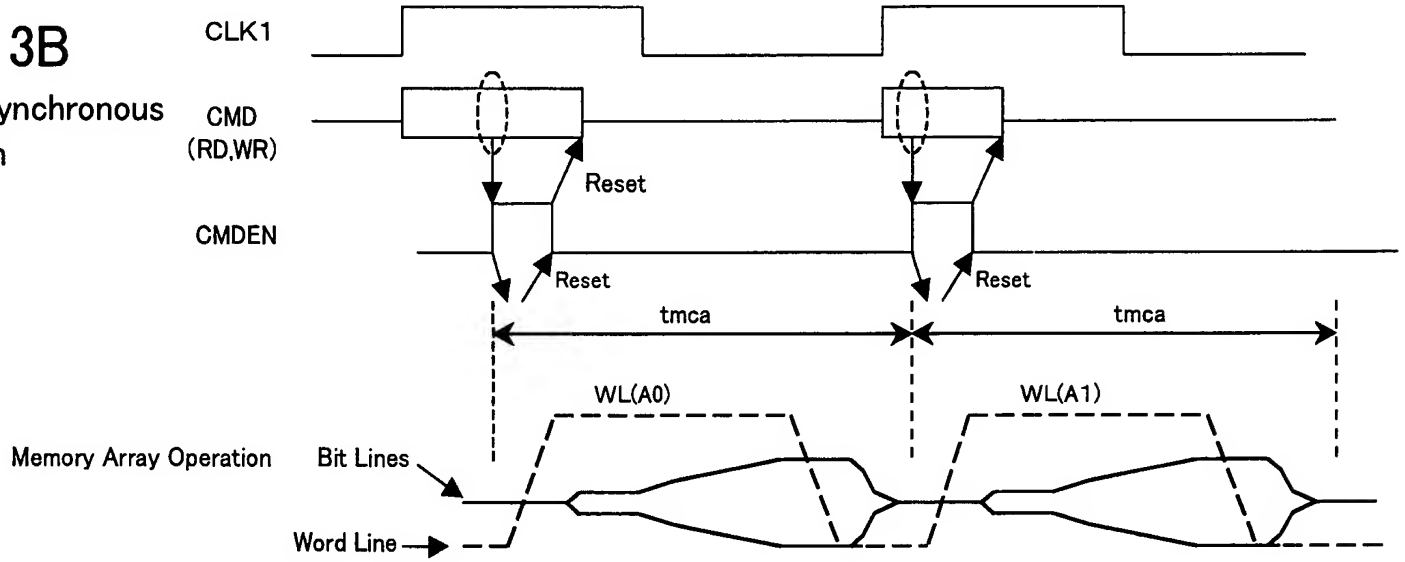


FIG. 4

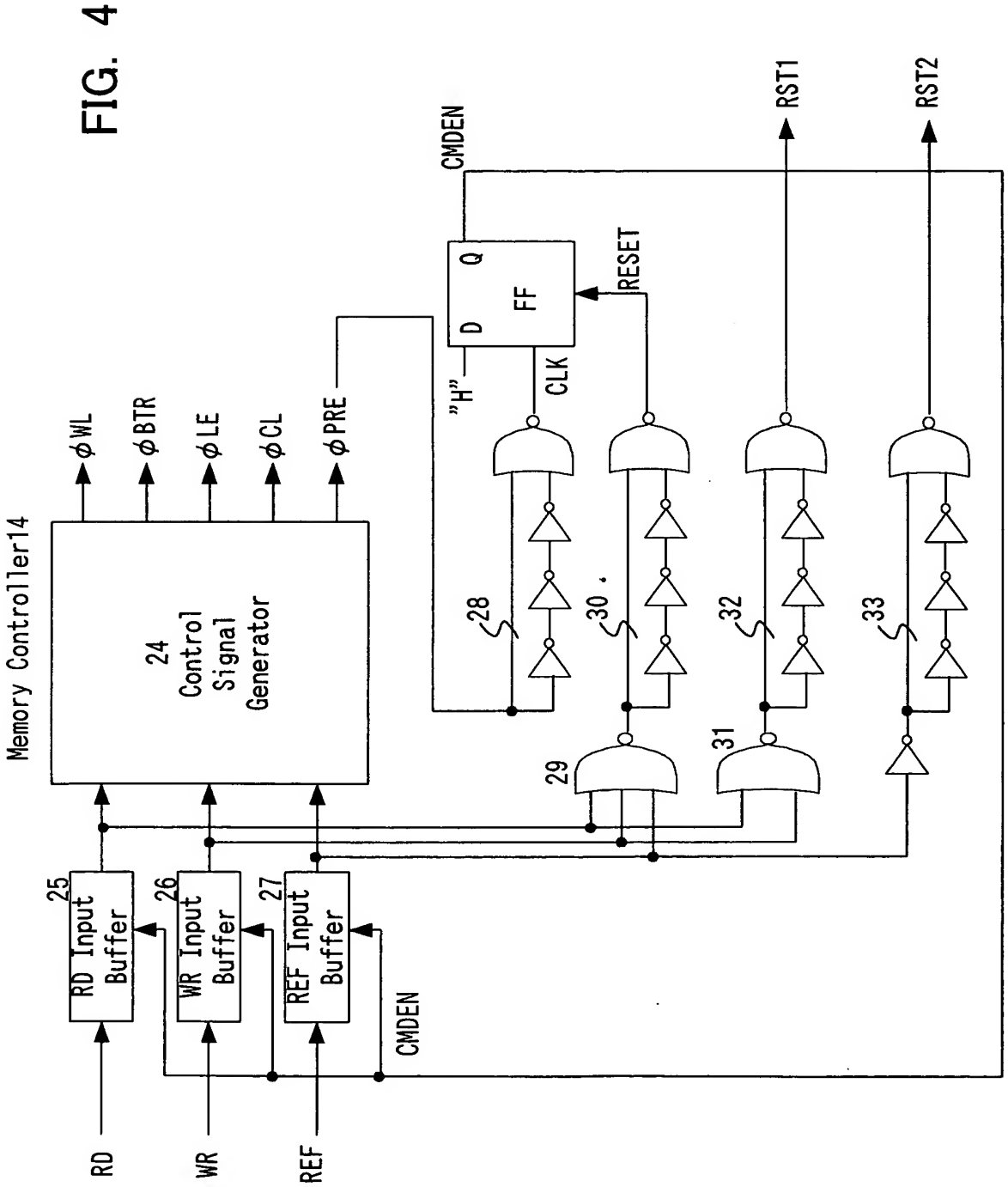

Memory Controller14
24
Control
Signal
Generator
φWL
φBTR
φLE
φCL
φPRE
RD
WR
REF
25
RD Input
Buffer
26
WR Input
Buffer
27
REF Input
Buffer
CMDEN
"H"
D
Q
FF
CLK
RESET
CMDEN
RST1
RST2
28
29
30
31
32
33

FIG. 5

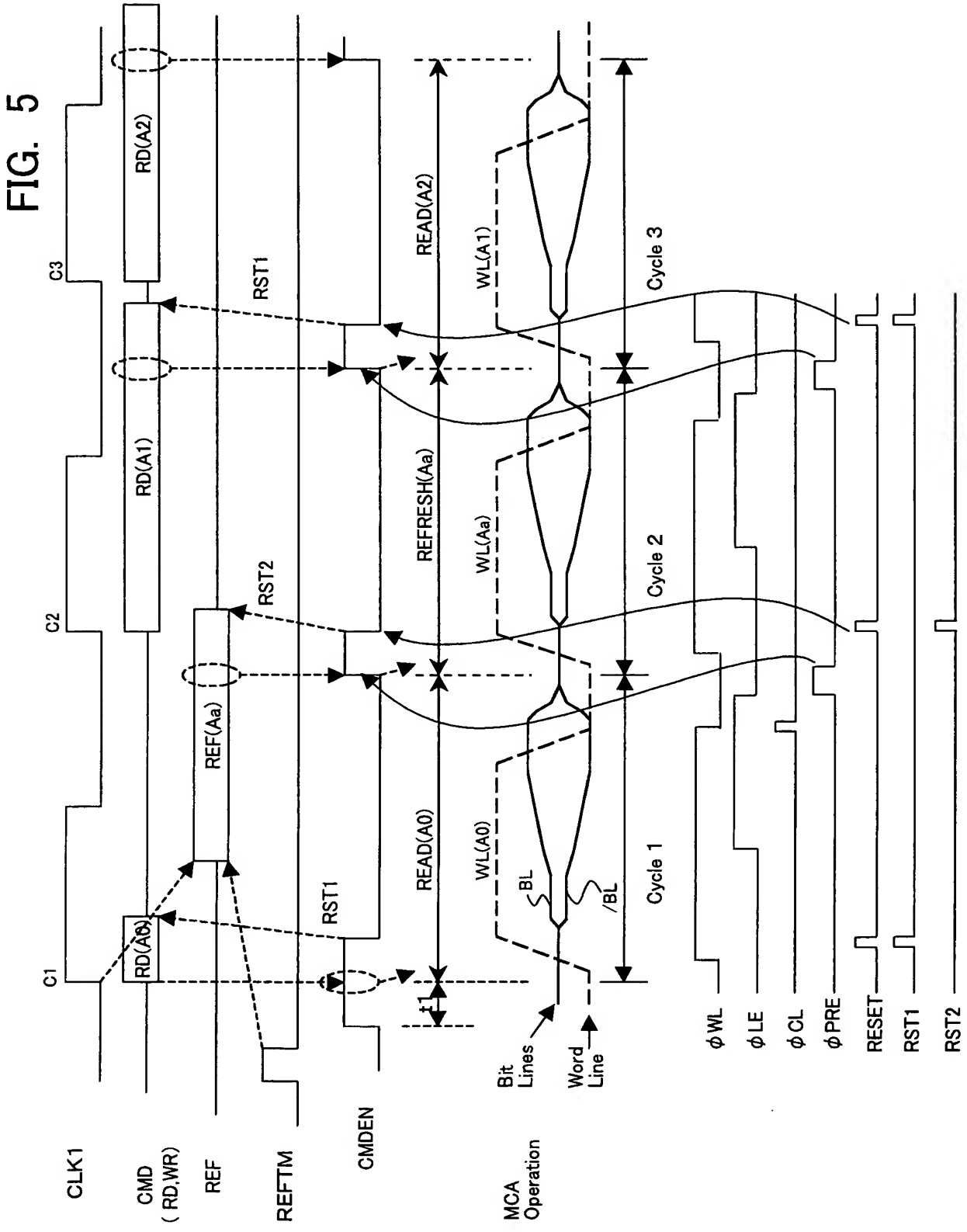

CLK1
CMD (RD,WR)
REF
REFTM
CMDEN
MCA Operation
C1
C2
C3
RD(A0)
RD(A1)
RD(A2)
REF(Aa)
RST1
RST2
RST1
RST1
READ(A0)
REFRESH(Aa)
READ(A2)
t1
WL(A0)
WL(Aa)
WL(A1)
BL
/BL
Bit Lines
Word Line
Cycle 1
Cycle 2
Cycle 3
φWL
φLE
φCL
φPRE
RESET
RST1
RST2

FIG. 6

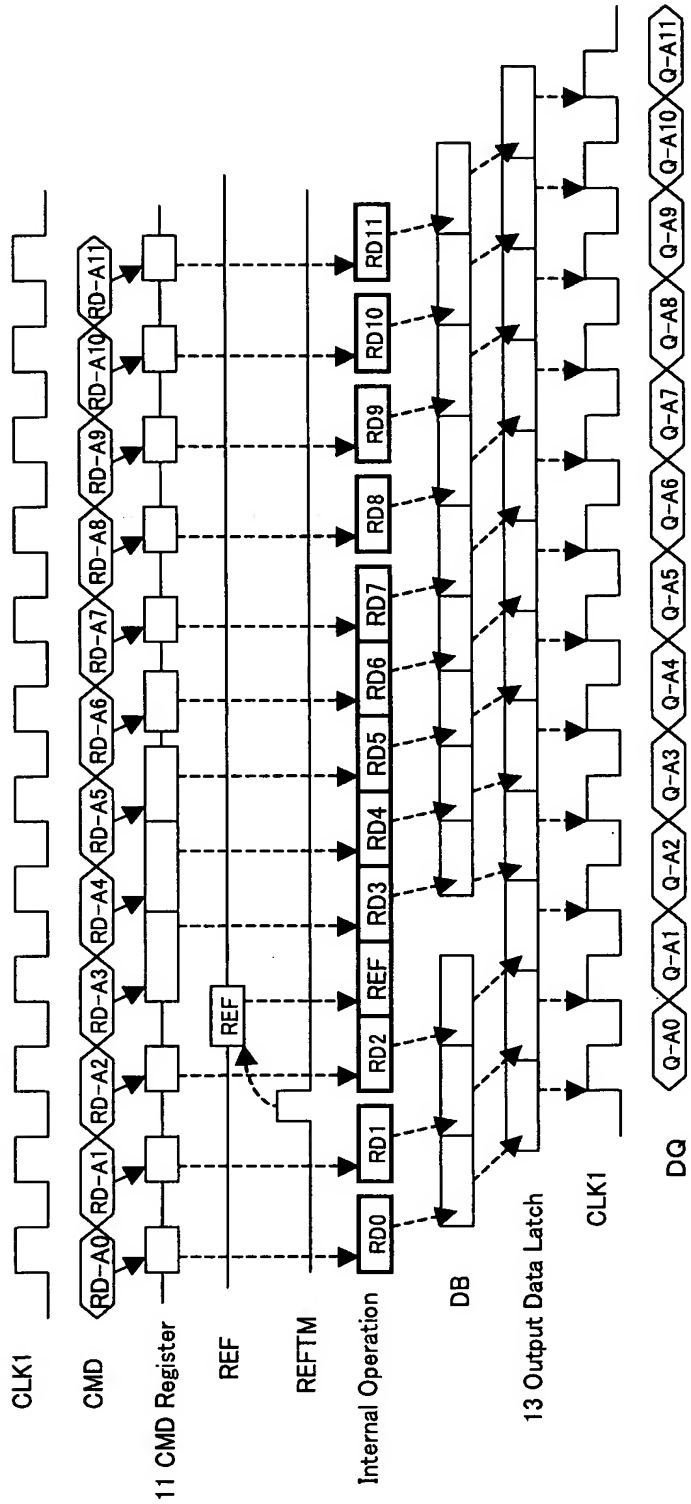

CLK1
CMD
11 CMD Register
REF
REFTM
Internal Operation
DB
13 Output Data Latch
CLK1
DQ
RD-A0
RD-A1
RD-A2
RD-A3
RD-A4
RD-A5
RD-A6
RD-A7
RD-A8
RD-A9
RD-A10
RD-A11
REF
RD0
RD1
RD2
REF
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
Q-A0
Q-A1
Q-A2
Q-A3
Q-A4
Q-A5
Q-A6
Q-A7
Q-A8
Q-A9
Q-A10
Q-A11

FIG. 7

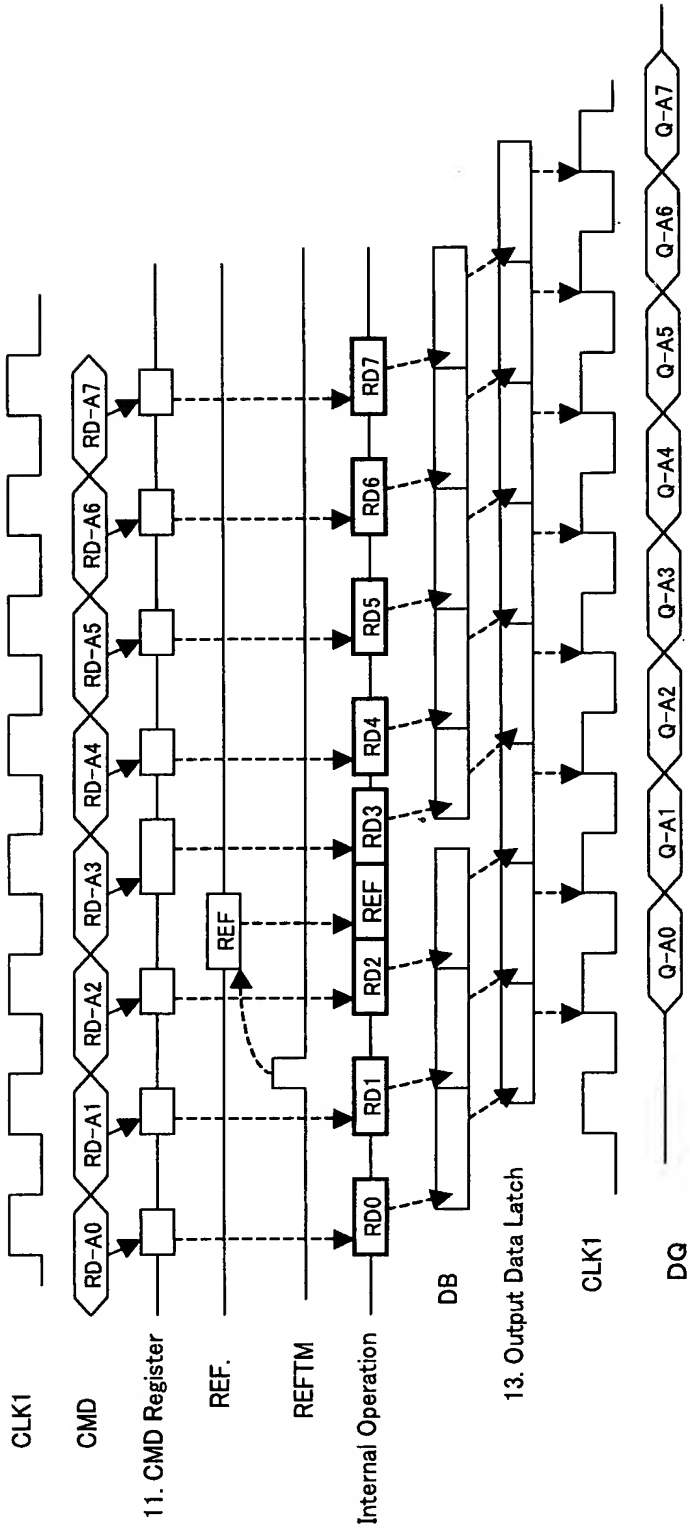

CLK1
CMD
RD-A0
RD-A1
RD-A2
RD-A3
RD-A4
RD-A5
RD-A6
RD-A7
11. CMD Register
REF.
REF
REFTM
Internal Operation
RD0
RD1
RD2
REF
RD3
RD4
RD5
RD6
RD7
DB
13. Output Data Latch
CLK1
DQ
Q-A0
Q-A1
Q-A2
Q-A3
Q-A4
Q-A5
Q-A6
Q-A7

FIG. 8

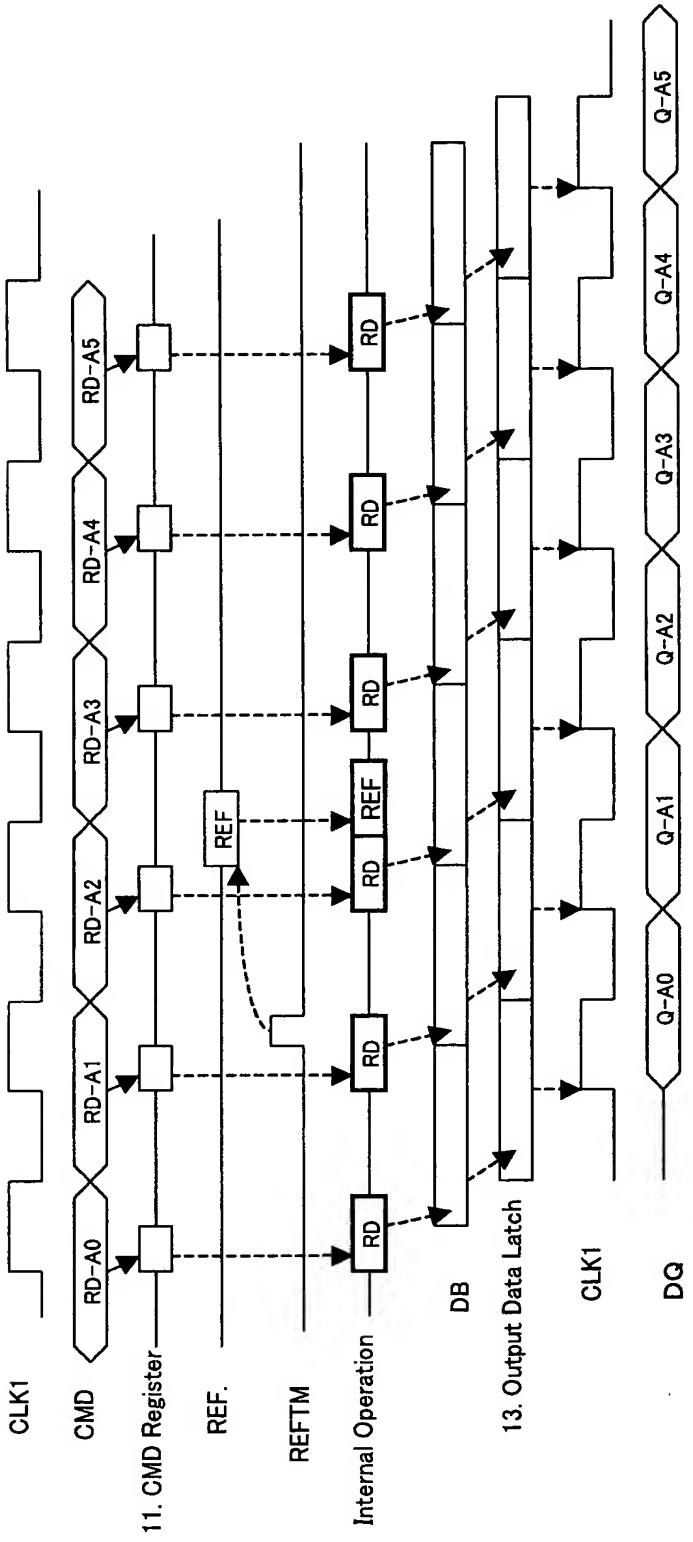

CLK1
CMD
11. CMD Register
REF.
REFTM
Internal Operation
DB
13. Output Data Latch
CLK1
DQ
RD-A0
RD-A1
RD-A2
RD-A3
RD-A4
RD-A5
REF
RD
Q-A0
Q-A1
Q-A2
Q-A3
Q-A4
Q-A5

FIG. 9

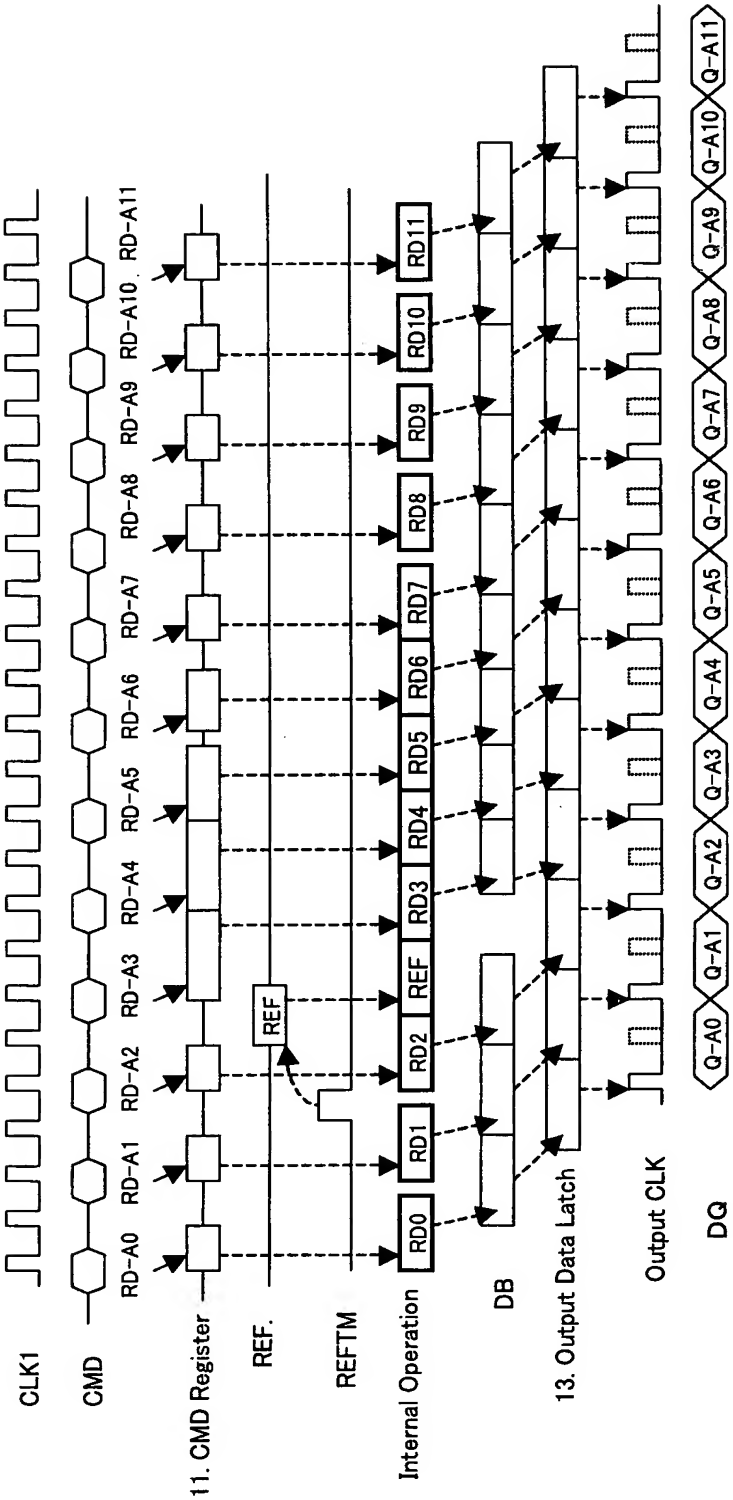

CLK1
CMD
RD-A0
RD-A1
RD-A2
RD-A3
RD-A4
RD-A5
RD-A6
RD-A7
RD-A8
RD-A9
RD-A10
RD-A11
11. CMD Register
REF.
REFTM
Internal Operation
RD0
RD1
RD2
REF
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
DB
13. Output Data Latch
Output CLK
DQ
Q-A0
Q-A1
Q-A2
Q-A3
Q-A4
Q-A5
Q-A6
Q-A7
Q-A8
Q-A9
Q-A10
Q-A11

FIG. 10

Second Embodiment

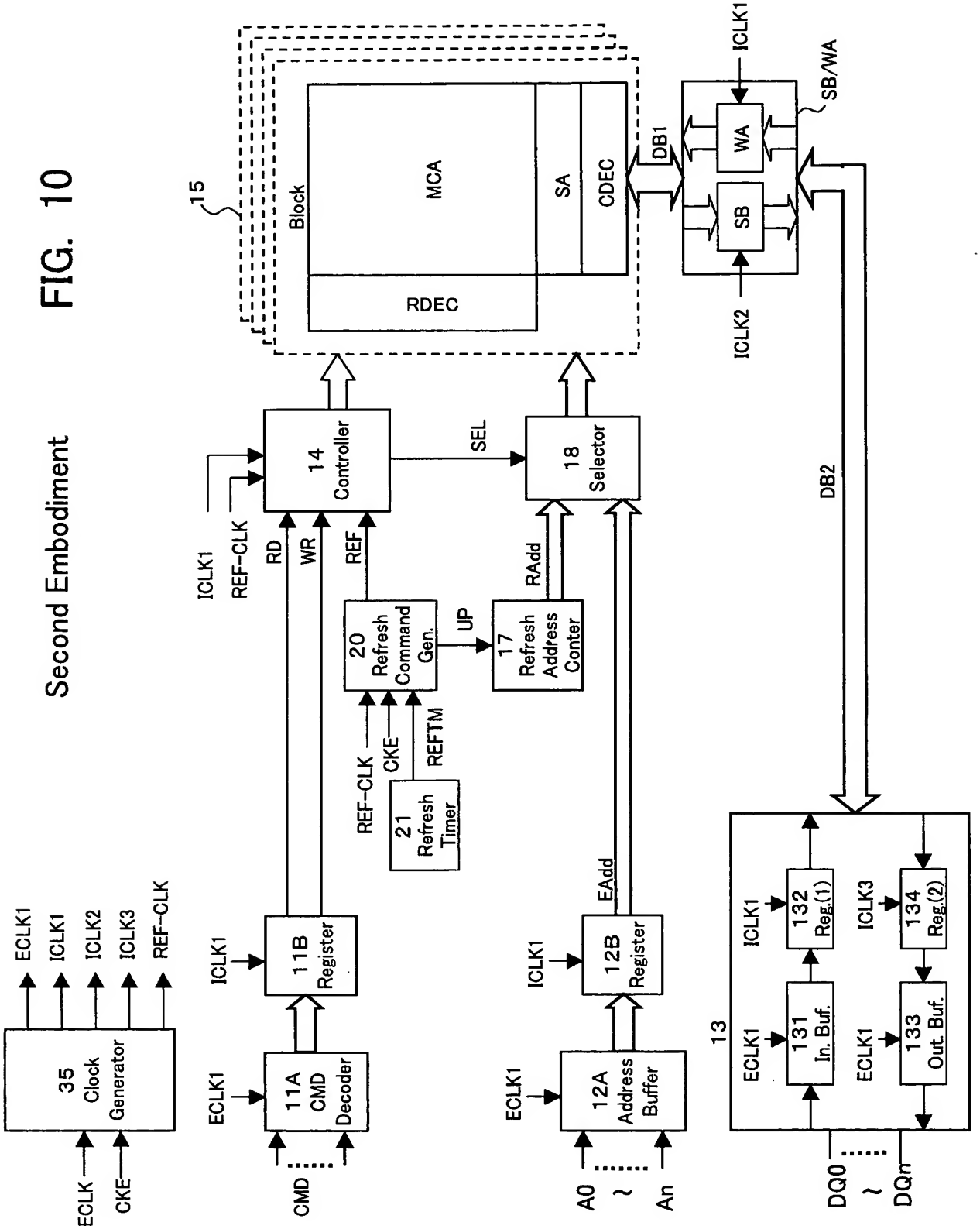


FIG. 11

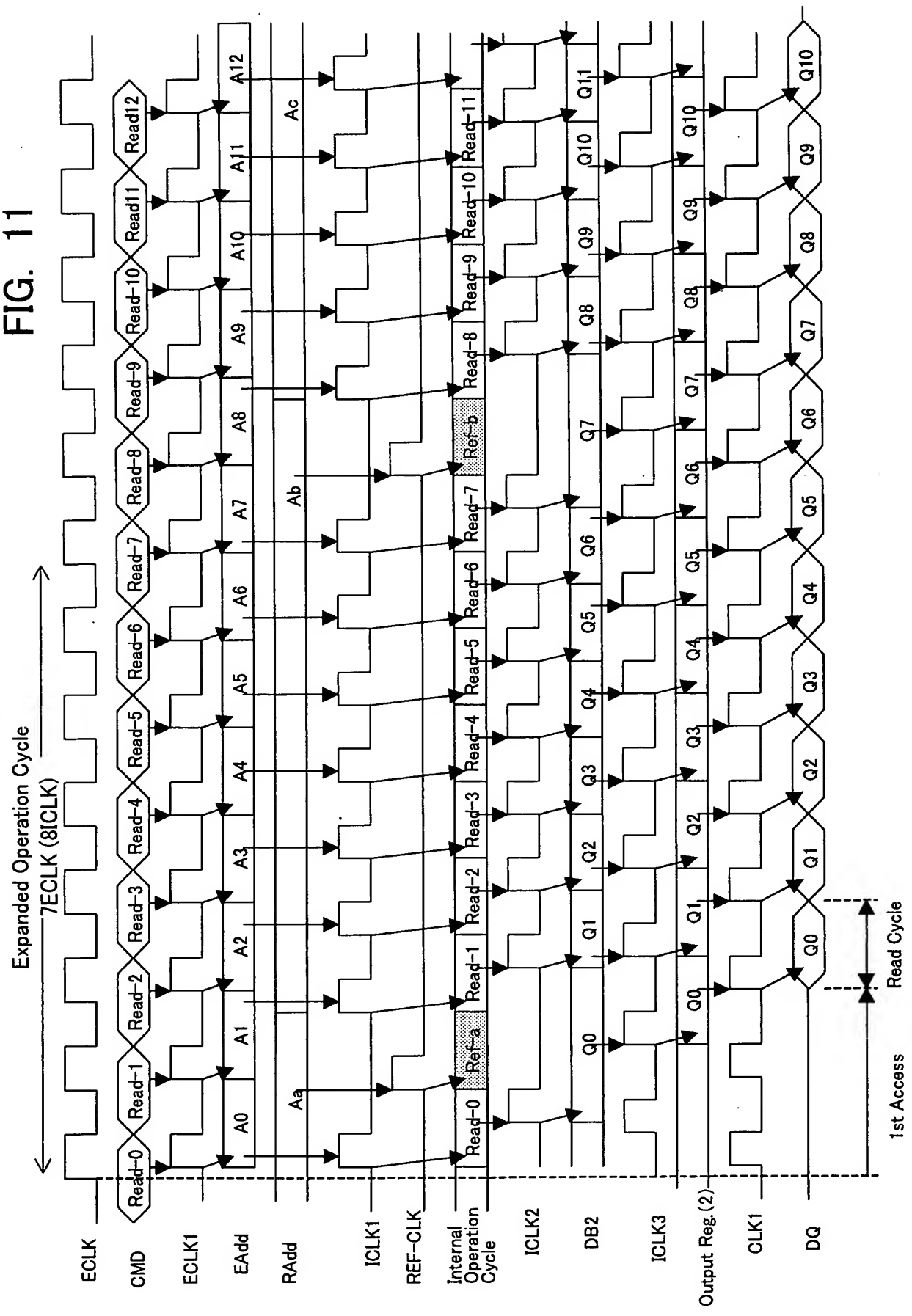

Expanded Operation Cycle
7ECLK (8ICLK)
ECLK
CMD
ECLK1
EAdd
RAdd
ICLK1
REF-CLK
Internal Operation Cycle
ICLK2
DB2
ICLK3
Output Reg. (2)
CLK1
DQ
Read-0
Read-1
Read-2
Read-3
Read-4
Read-5
Read-6
Read-7
Read-8
Read-9
Read-10
Read-11
Read12
Ref-a
Ref-b
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
Aa
Ab
Ac
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
1st Access
Read Cycle

FIG. 12

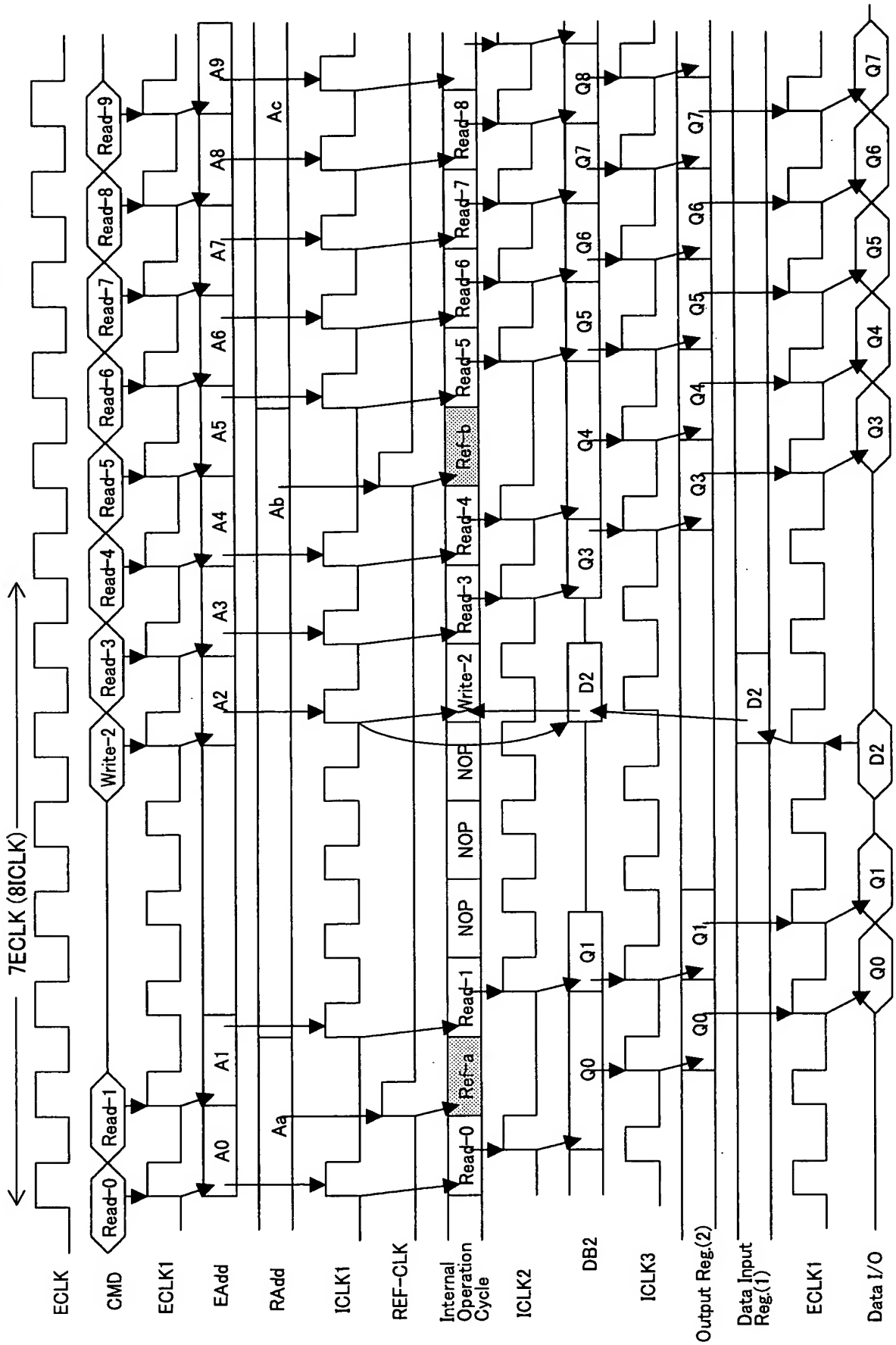

7ECLK (8ICLK)
ECLK
CMD
ECLK1
EAdd
RAdd
ICLK1
REF-CLK
Internal Operation Cycle
ICLK2
DB2
ICLK3
Output Reg.(2)
Data Input Reg.(1)
ECLK1
Data I/O
Read-0
Read-1
Write-2
Read-3
Read-4
Read-5
Read-6
Read-7
Read-8
Read-9
Ref-a
Ref-b
NOP
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
Aa
Ab
Ac
D2
Q0
Q1
Q3
Q4
Q5
Q6
Q7
Q8

FIG. 13

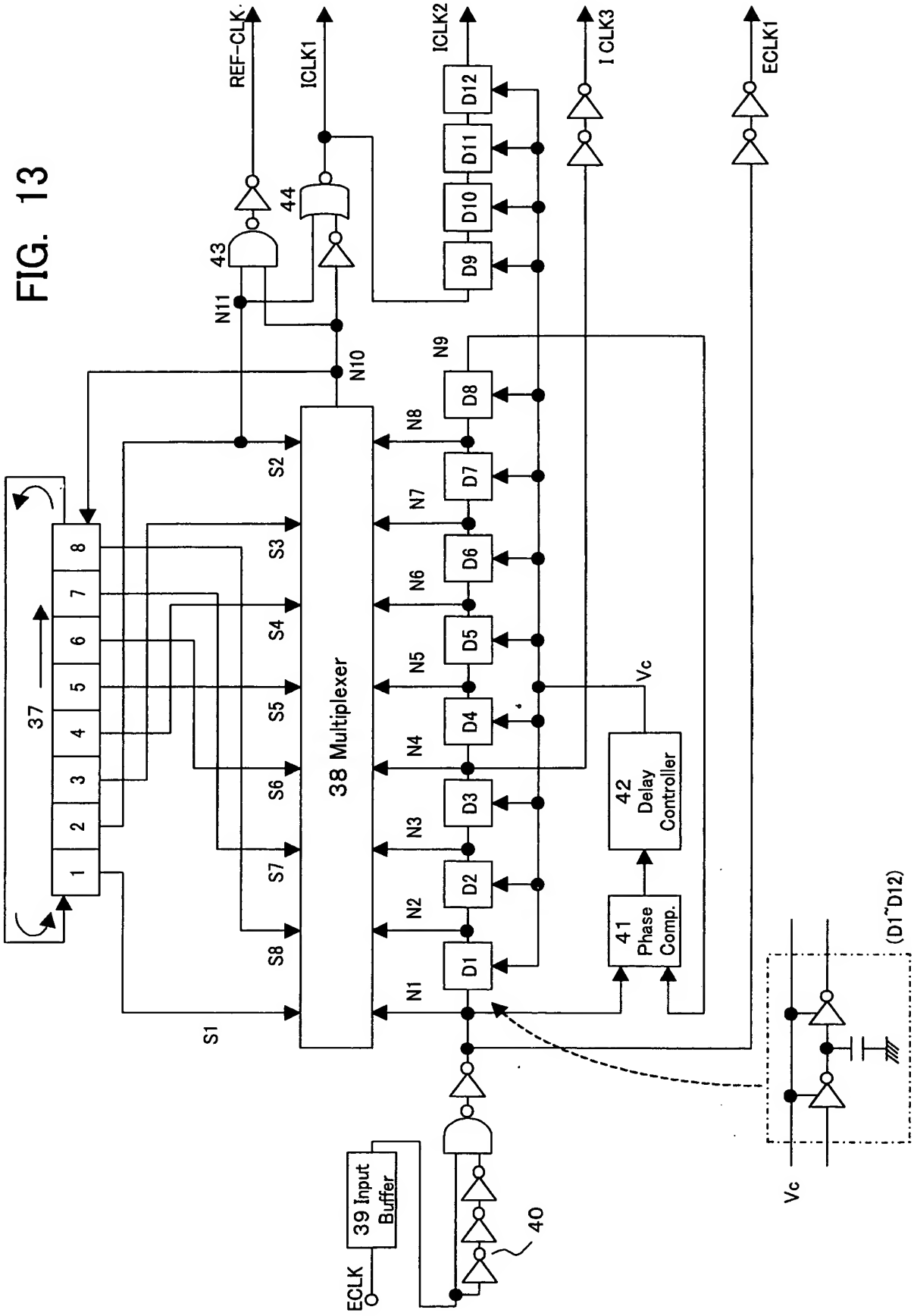

REF-CLK
ICLK1
ICLK2
I CLK3
ECLK1
43
44
N11
N10
N9
N8
N7
N6
N5
N4
N3
N2
N1
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
S1
S2
S3
S4
S5
S6
S7
S8
37
1
2
3
4
5
6
7
8
38 Multiplexer
42 Delay Controller
41 Phase Comp.
Vc
39 Input Buffer
ECLK
40
(D1~D12)

FIG. 14

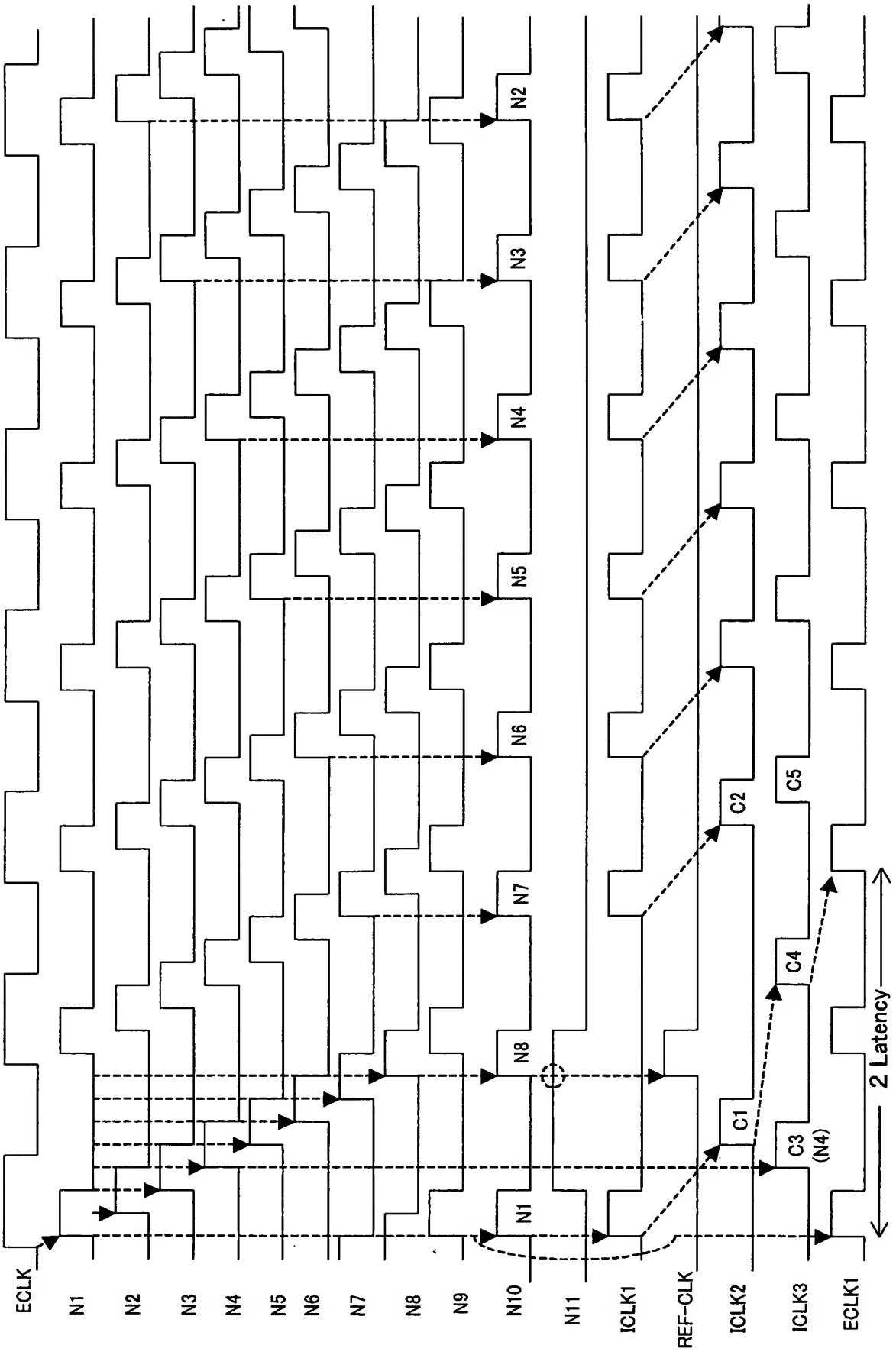
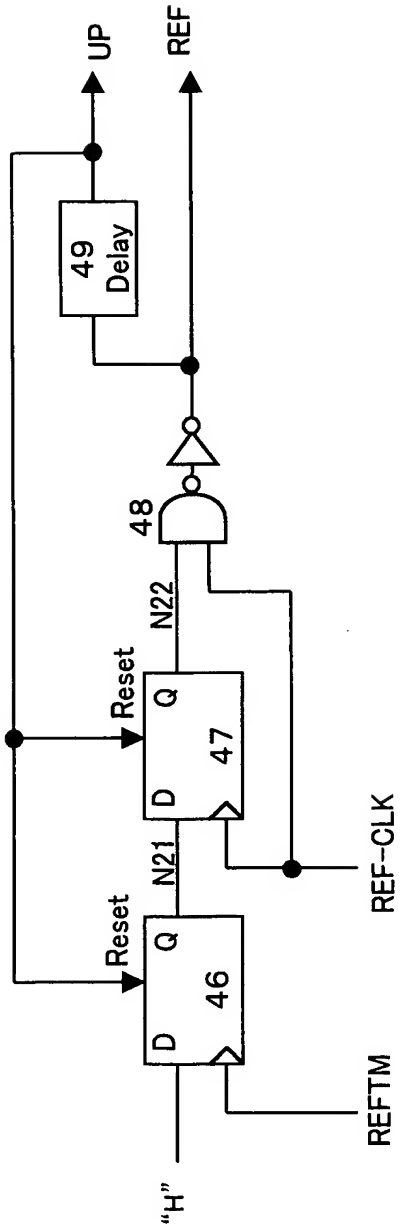

ECLK
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
ICLK1
REF-CLK
ICLK2
ICLK3
ECLK1
C1
C2
C3
(N4)
C4
C5
2 Latency

FIG. 15

Refresh Command Generator



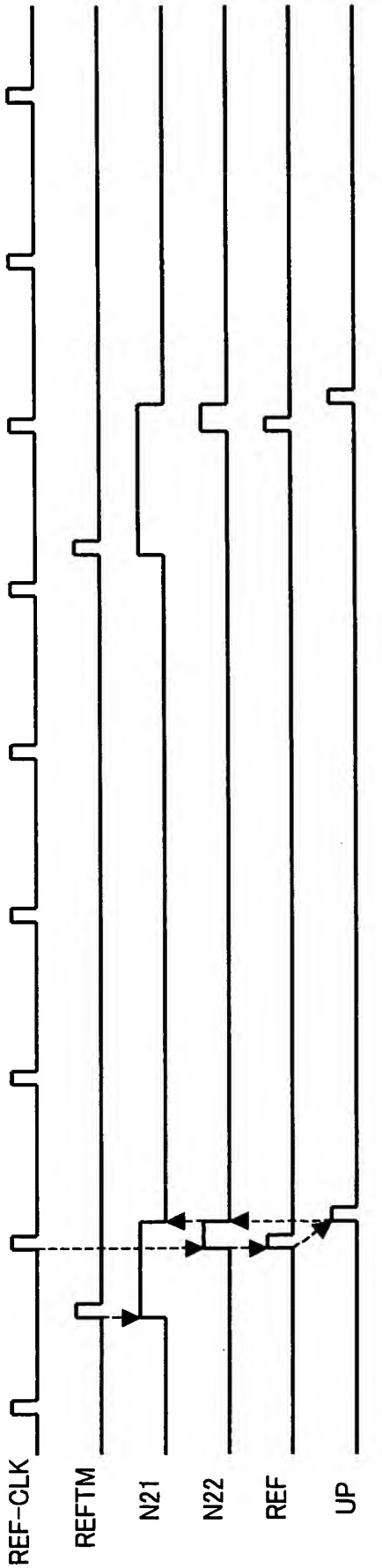


FIG. 16

Third Embodiment

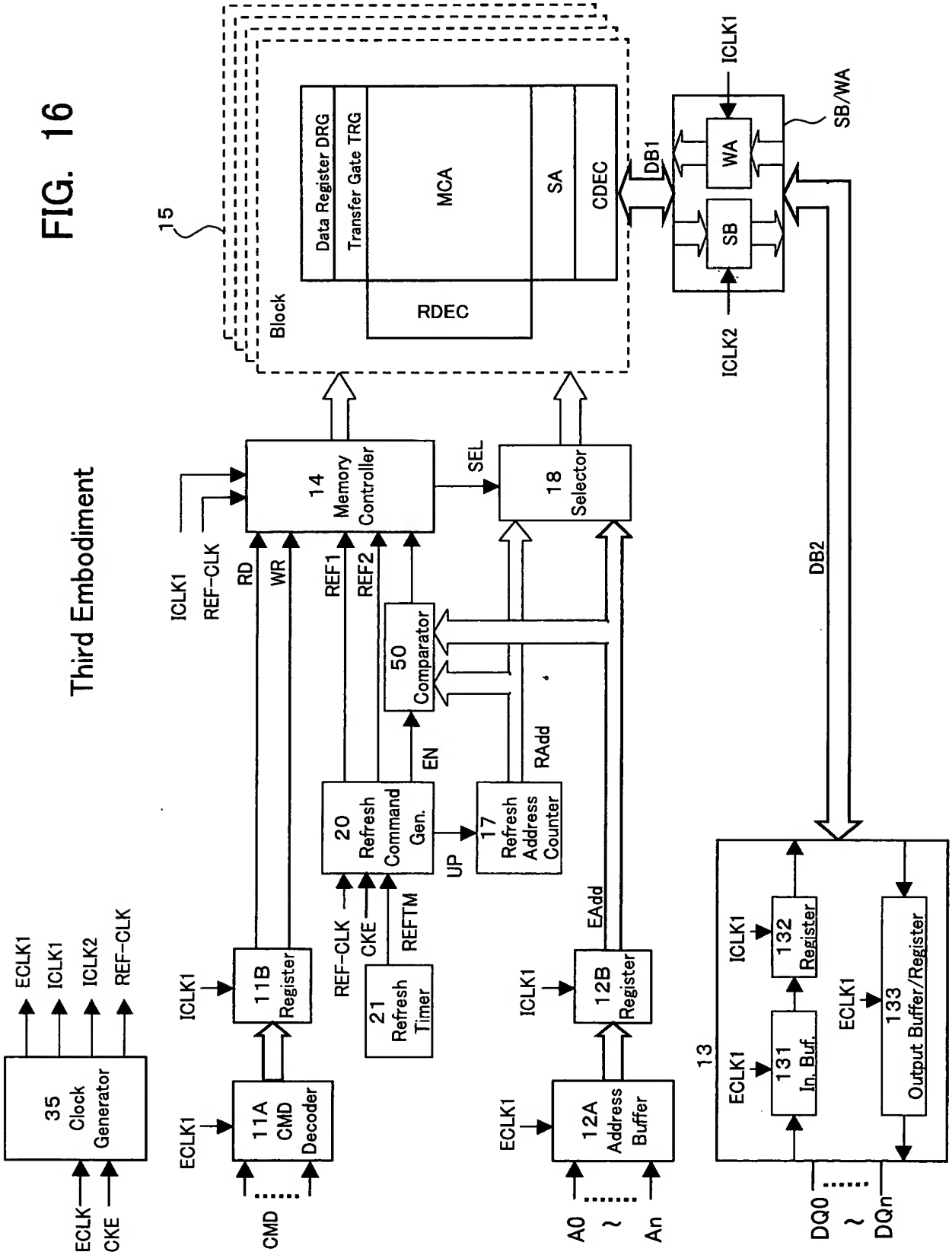


FIG. 17A
Normal Refresh Operation

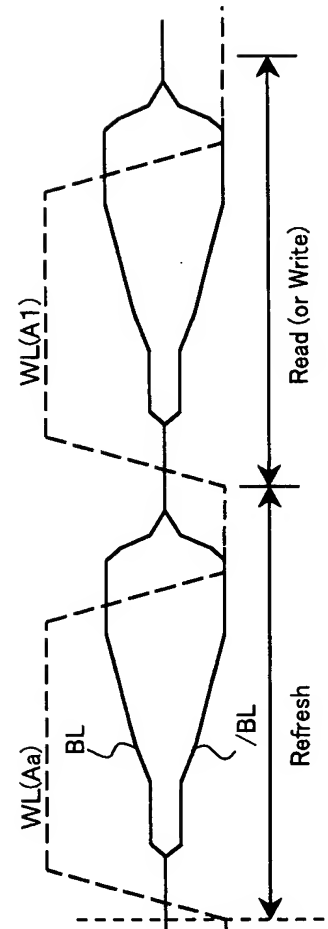


FIG. 17B
Refresh Operation (1)

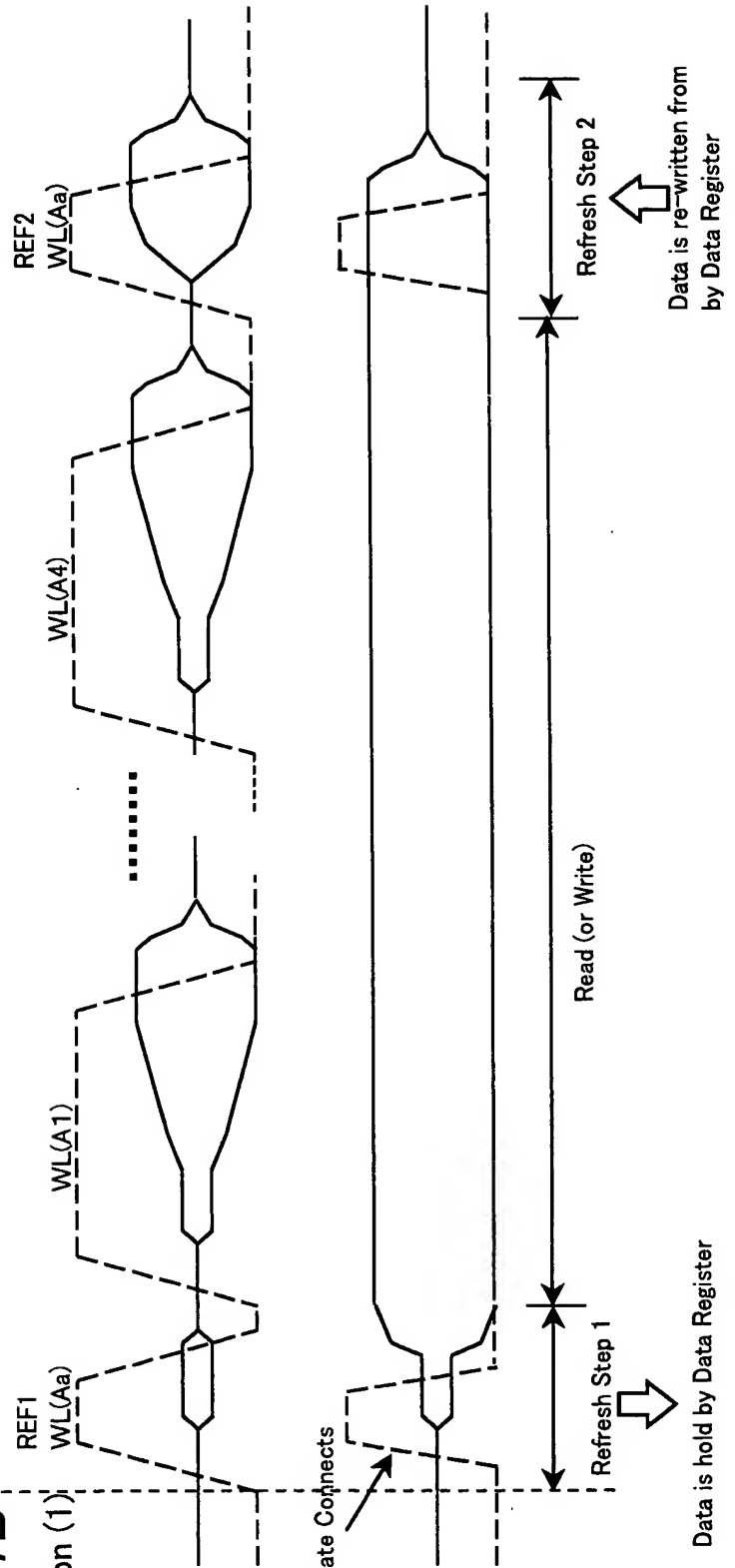


FIG. 18

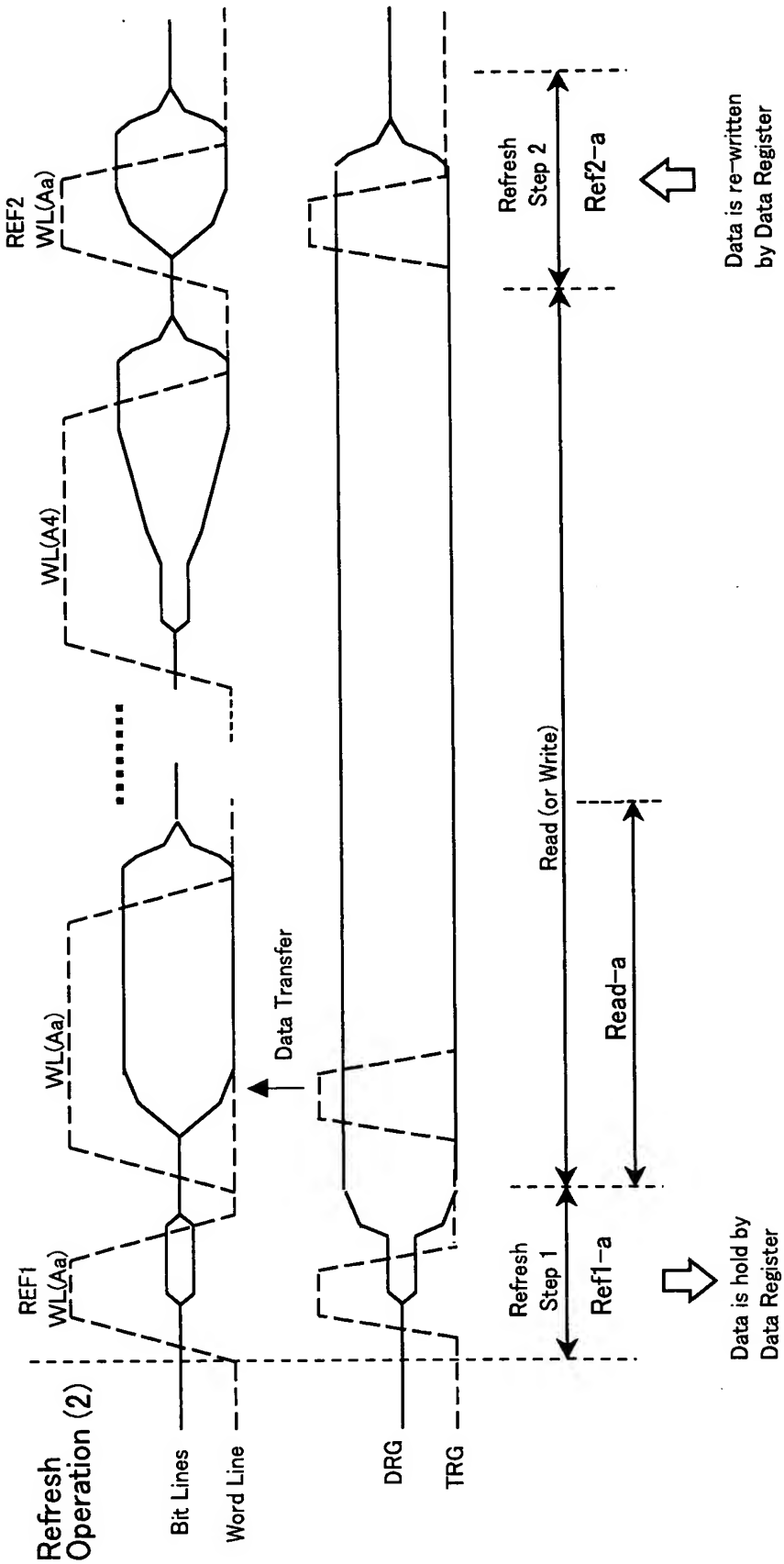

Refresh Operation (2)
Bit Lines
Word Line
REF1
WL(Aa)
WL(Aa)
Data Transfer
WL(A4)
REF2
WL(Aa)
DRG
TRG
Refresh Step 1
Ref1-a
Read-a
Read (or Write)
Refresh Step 2
Ref2-a
Data is hold by Data Register
Data is re-written by Data Register

FIG. 19

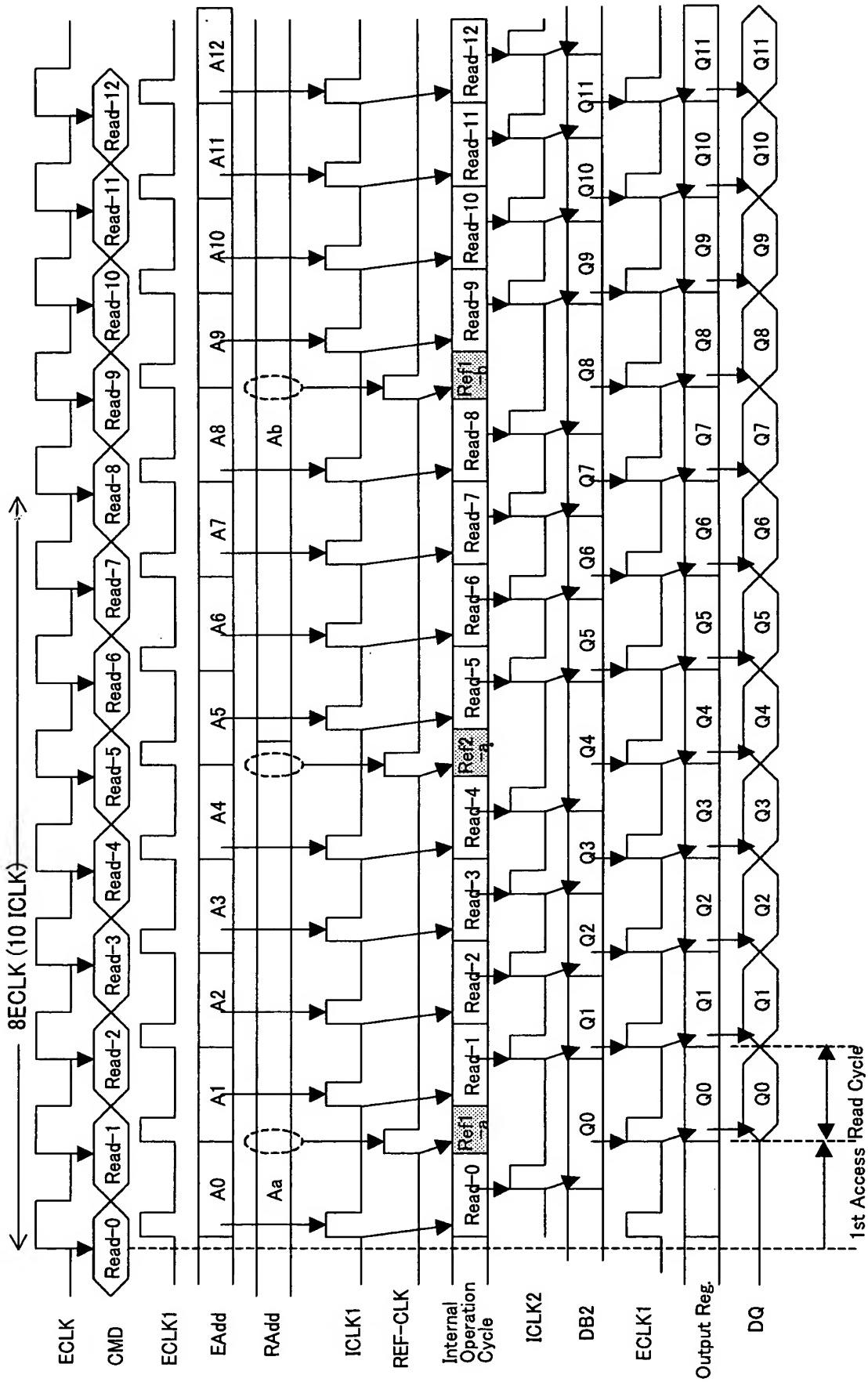

8ECLK (10 ICLK)
ECLK
CMD
ECLK1
EAdd
RAdd
ICLK1
REF-CLK
Internal Operation Cycle
ICLK2
DB2
ECLK1
Output Reg.
DQ
Read-0
Read-1
Read-2
Read-3
Read-4
Read-5
Read-6
Read-7
Read-8
Read-9
Read-10
Read-11
Read-12
Ref1_a
Ref2_a
Ref1_b
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
Aa
Ab
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
1st Access
Read Cycle

FIG. 20

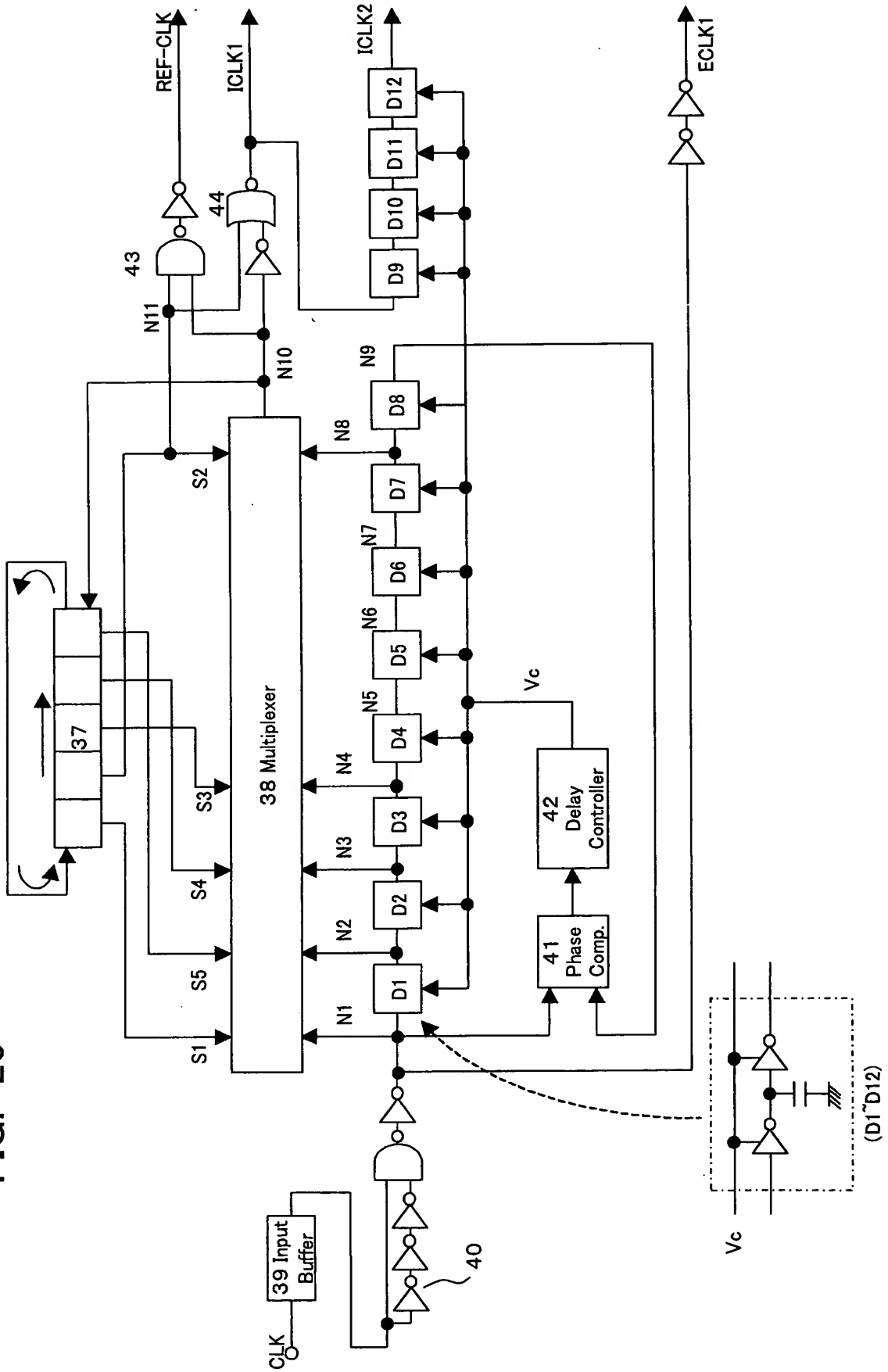

REF-CLK
ICLK1
ICLK2
ECLK1
43
44
N11
N10
N9
N8
N7
N6
N5
N4
N3
N2
N1
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
S1
S2
S3
S4
S5
37
38 Multiplexer
41 Phase Comp.
42 Delay Controller
Vc
39 Input Buffer
CLK
40
(D1~D12)

FIG. 21

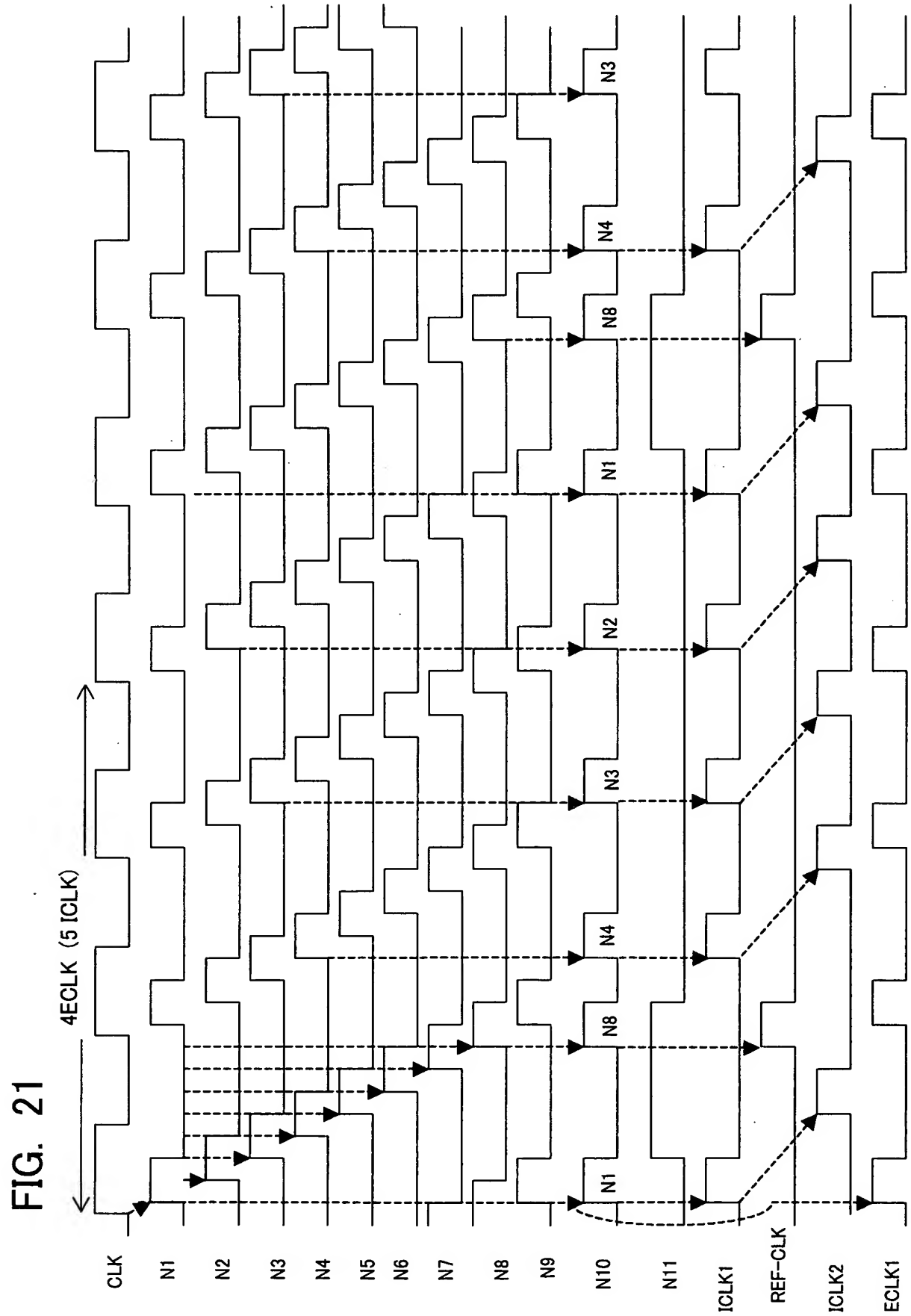

4ECLK (5 ICLK)
CLK
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
ICLK1
REF-CLK
ICLK2
ECLK1

FIG. 22

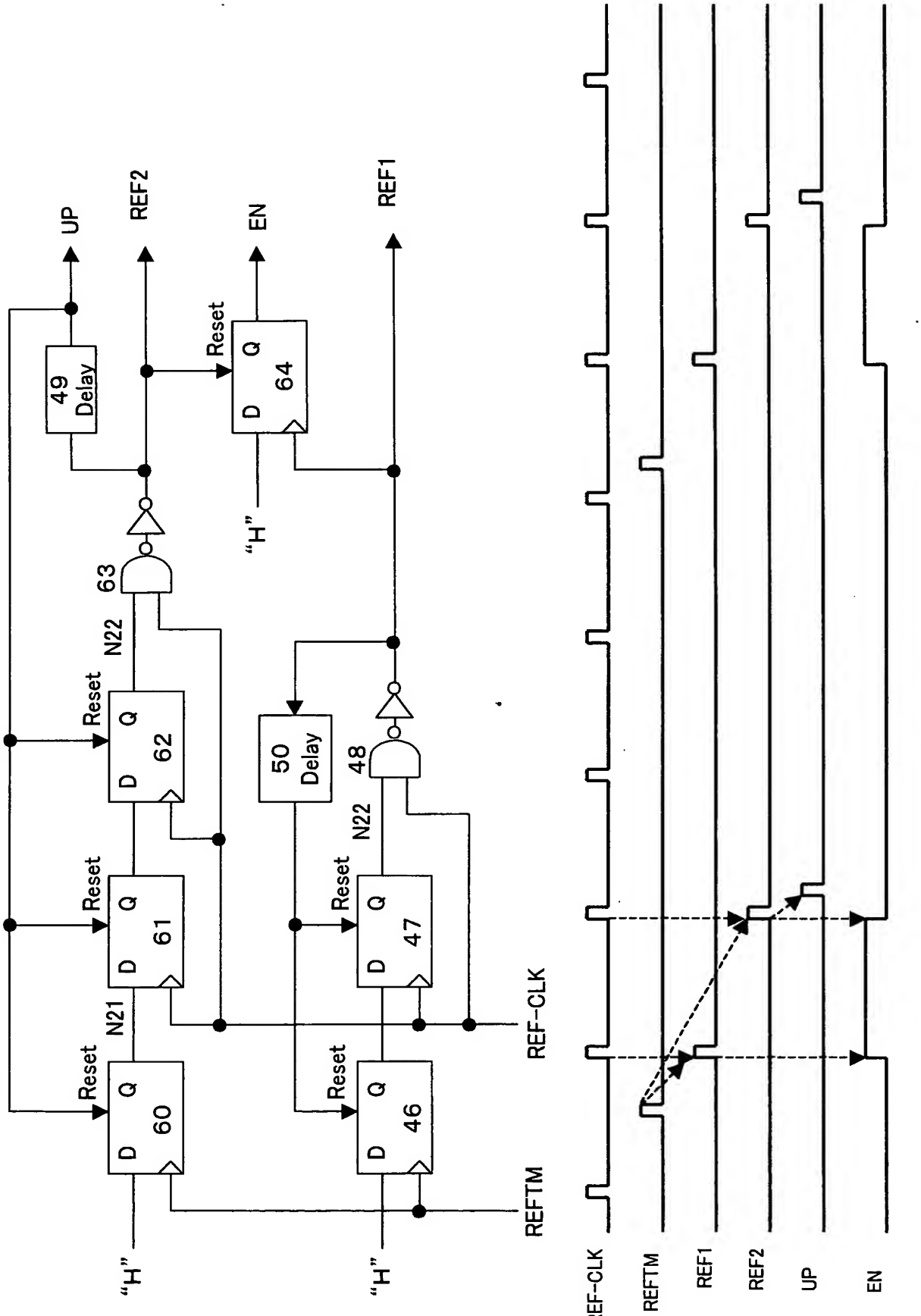
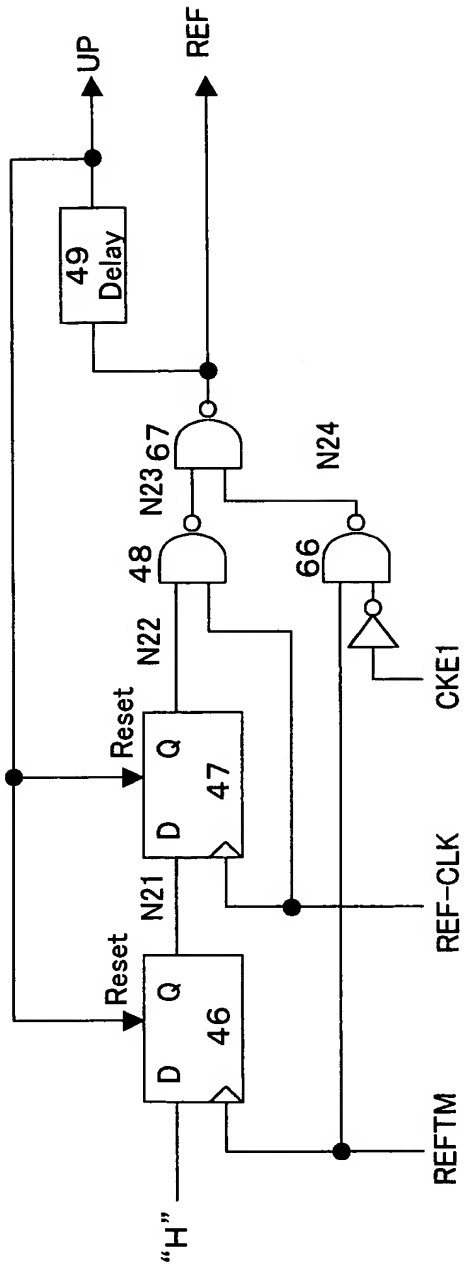

UP
REF2
EN
REF1
49 Delay
Reset
64
D
Q
"H"
63
N22
Reset
62
50 Delay
48
N22
Reset
61
Reset
47
N21
REF-CLK
Reset
60
Reset
46
REFTM
"H"
"H"
REF-CLK
REFTM
REF1
REF2
UP
EN

FIG. 23


UP
REF
49
Delay
67
N23
N24
48
66
N22
CKE1
Reset
Q
D
47
N21
REF-CLK
Reset
Q
D
46
REFTM
"H"

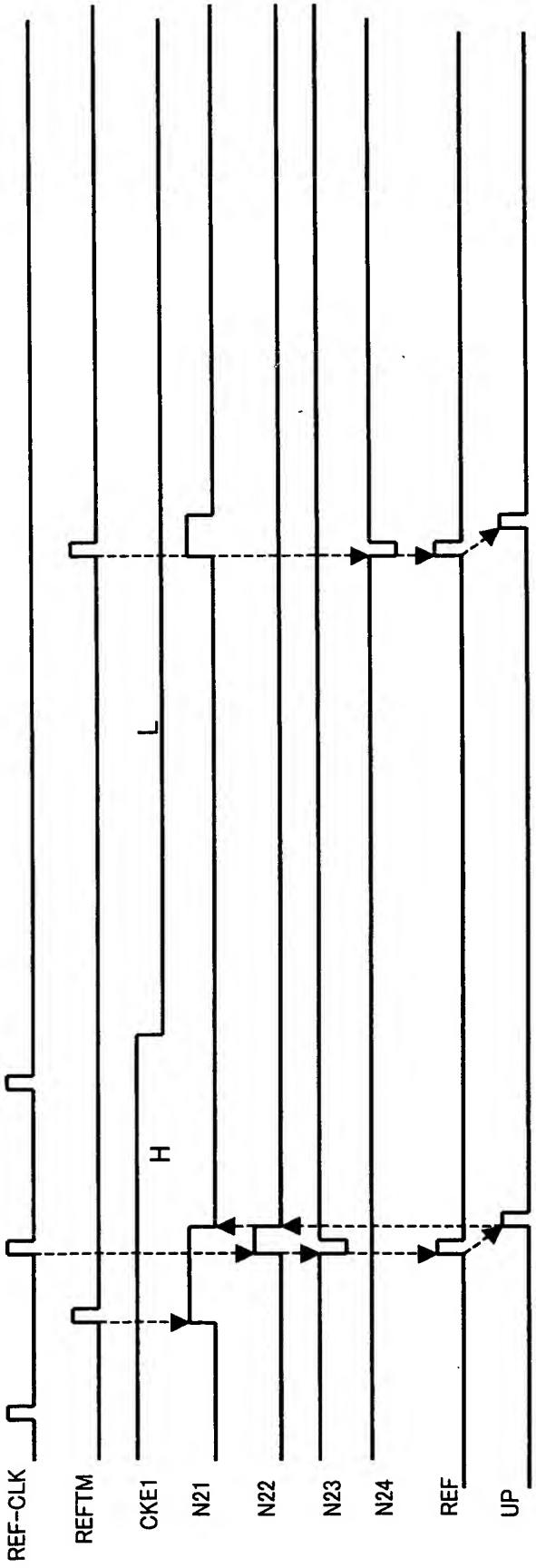

L
H
REF-CLK
REFTM
CKE1
N21
N22
N23
N24
REF
UP

FIG. 24
Fourth Embodiment

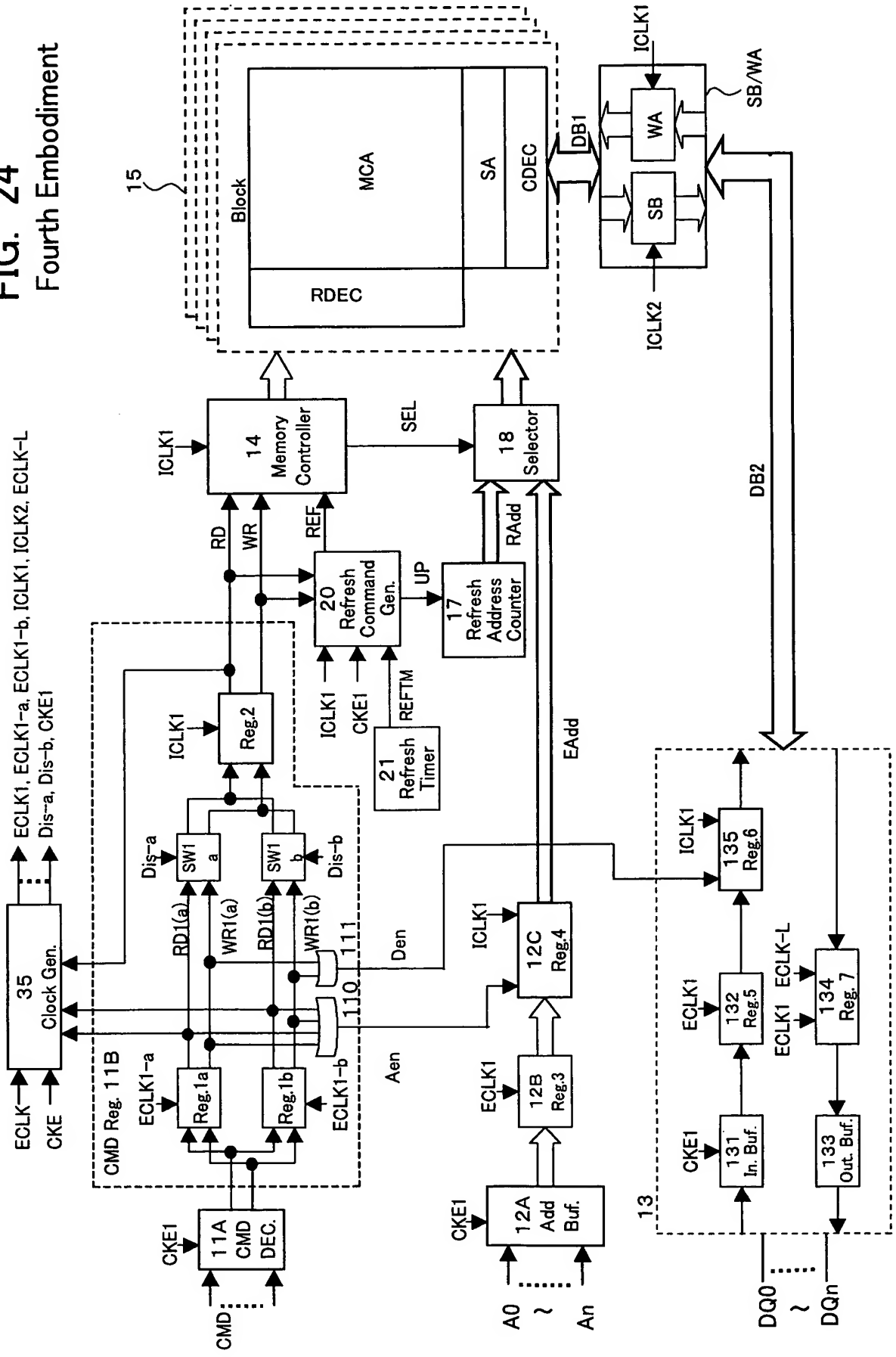


FIG. 25

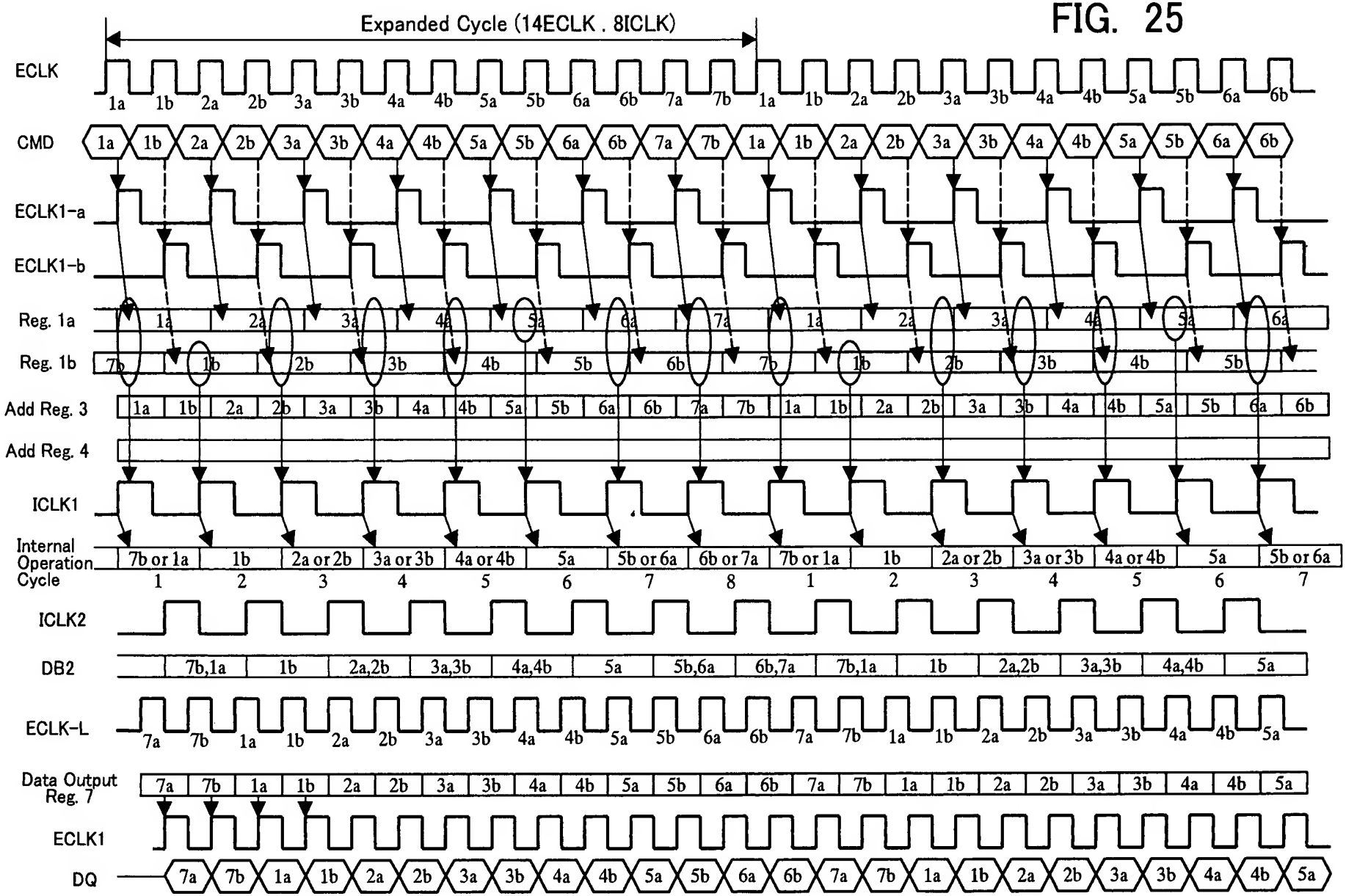


FIG. 26

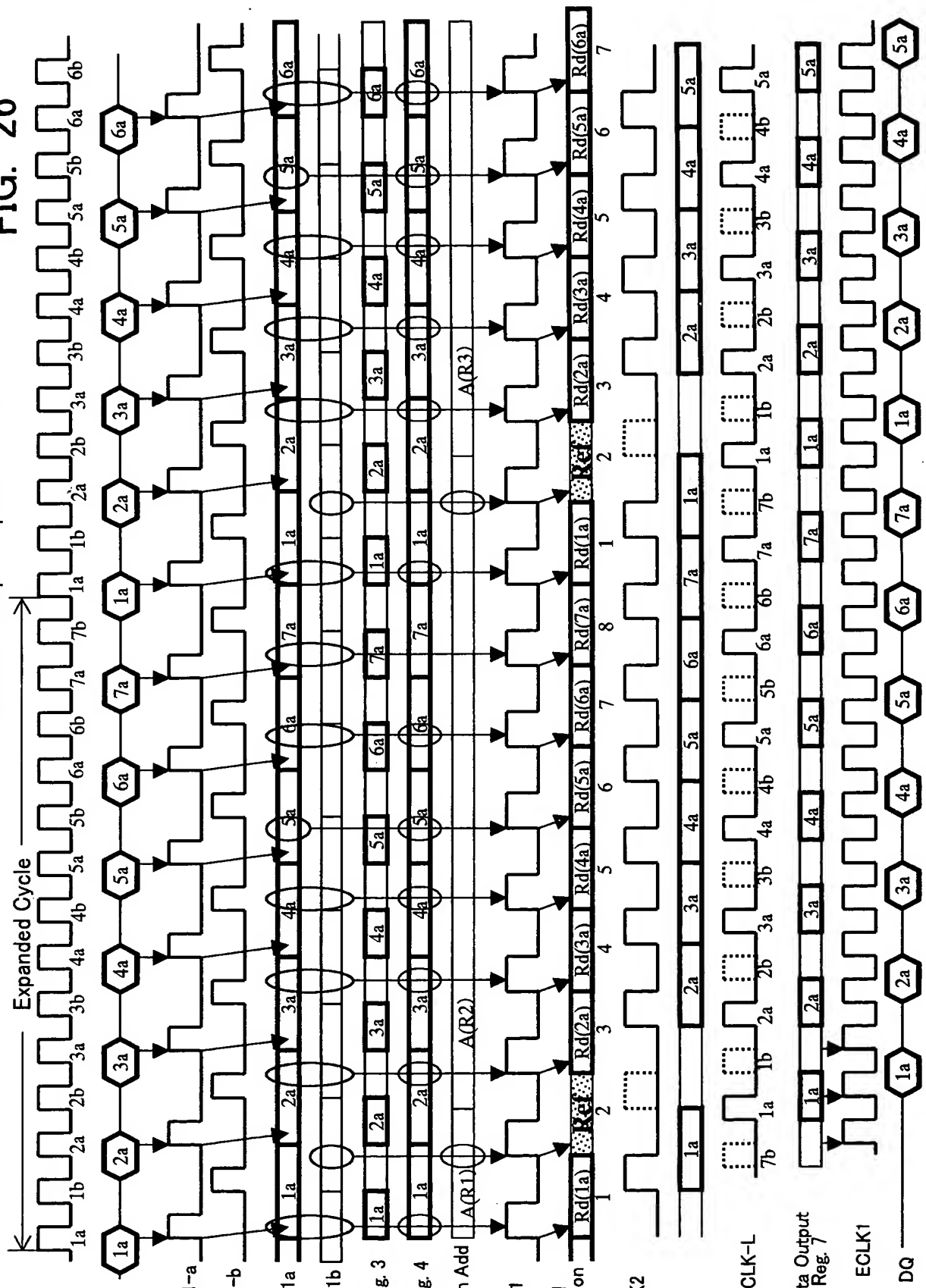

Command is input at phase "a" side
Expanded Cycle
ECLK
CMD
ECLK1-a
ECLK1-b
Reg. 1a
Reg. 1b
Add Reg. 3
Add Reg. 4
Refresh Add
ICLK1
Internal Operation Cycle
ICLK2
DB2
E CLK-L
Data Output Reg. 7
ECLK1
DQ
A(R1)
A(R2)
A(R3)
Ref
Rd(1a)
Rd(2a)
Rd(3a)
Rd(4a)
Rd(5a)
Rd(6a)
Rd(7a)

FIG. 27

Command is input at phase "b" side

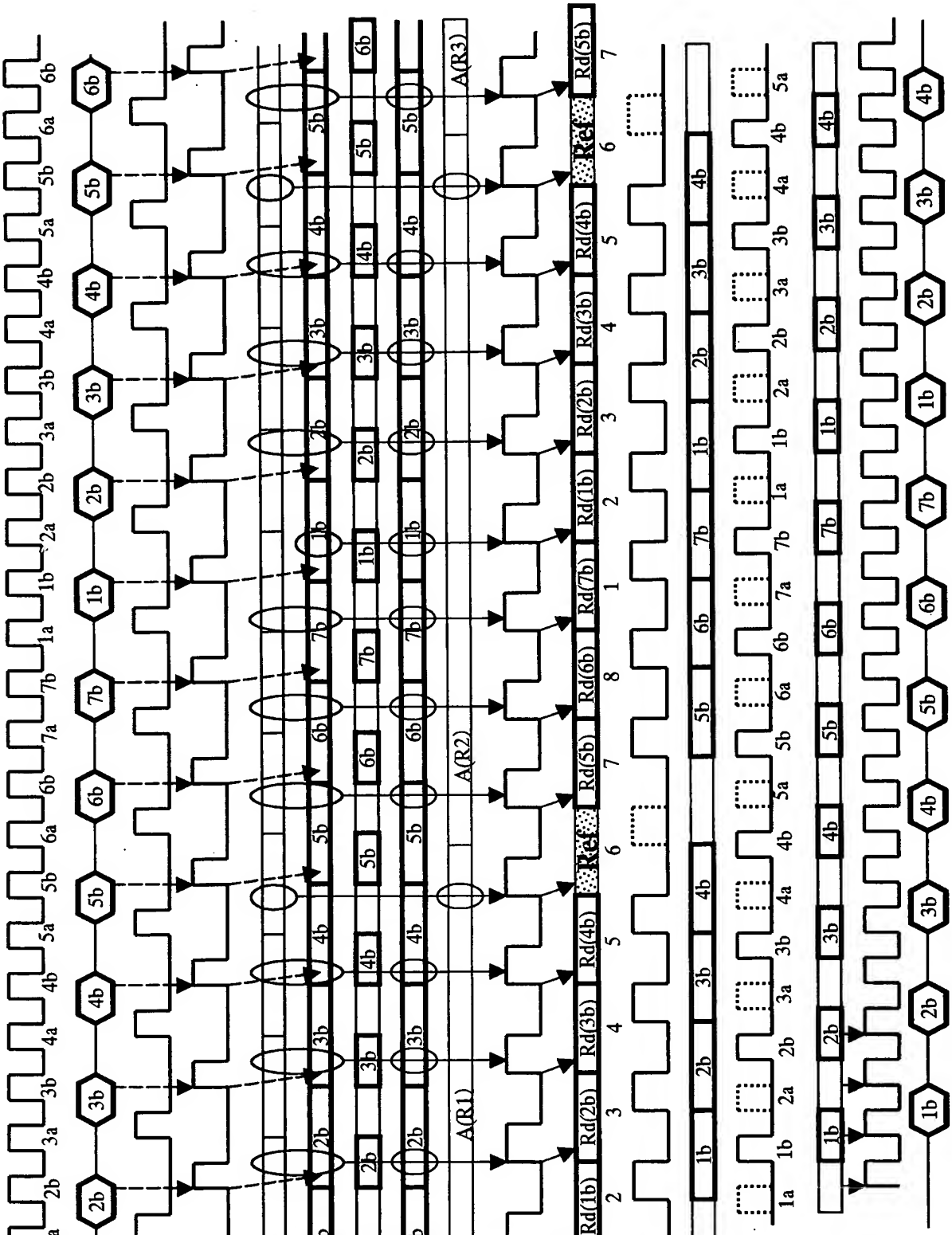


FIG. 28

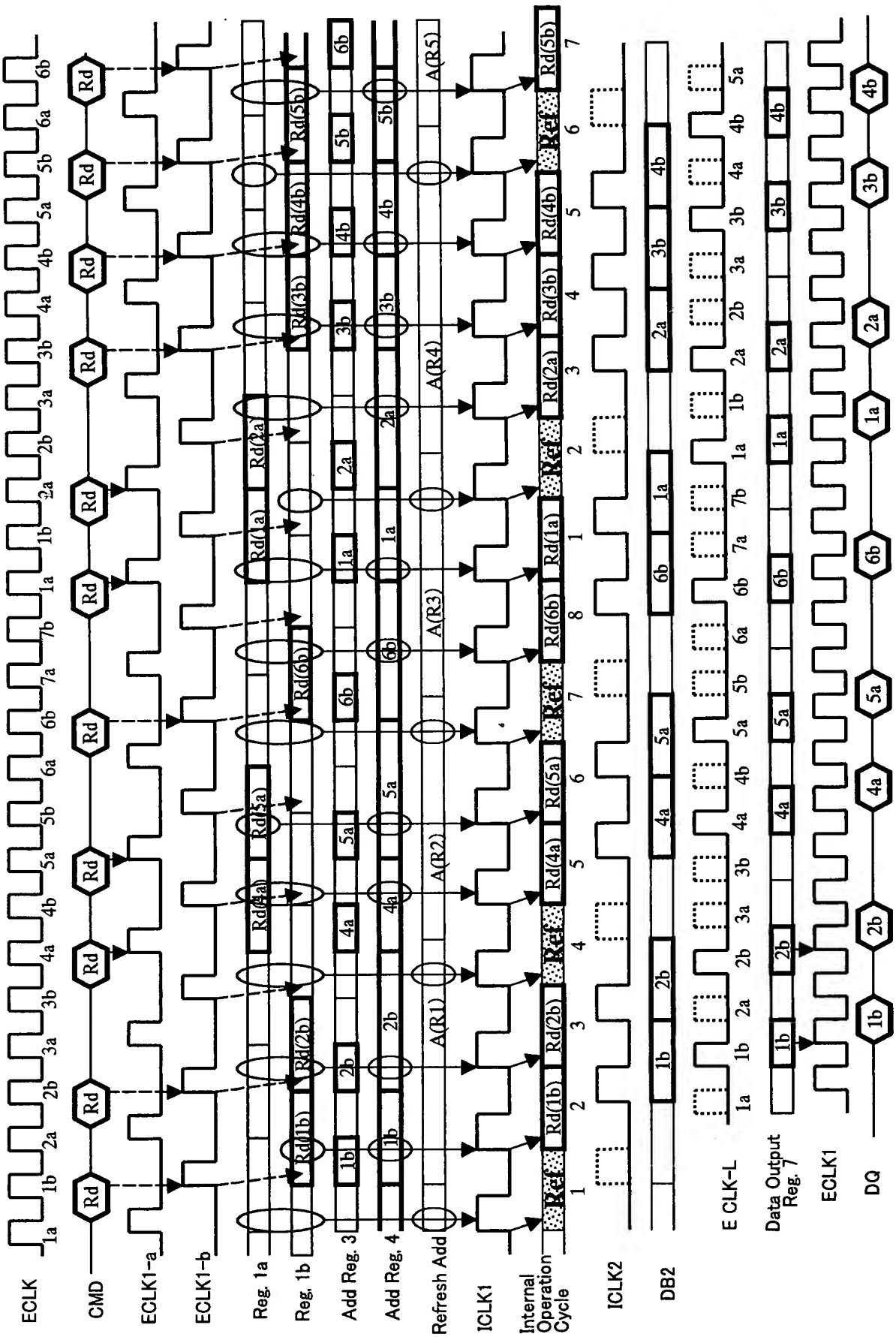

Command is input at phases "a" and "b" at random
ECLK
CMD
ECLK1-a
ECLK1-b
Reg. 1a
Reg. 1b
Add Reg. 3
Add Reg. 4
Refresh Add
ICLK1
Internal Operation Cycle
ICLK2
DB2
E CLK-L
Data Output Reg. 7
ECLK1
DQ
Rd
Ref
A(R1)
A(R2)
A(R3)
A(R4)
A(R5)

FIG. 29

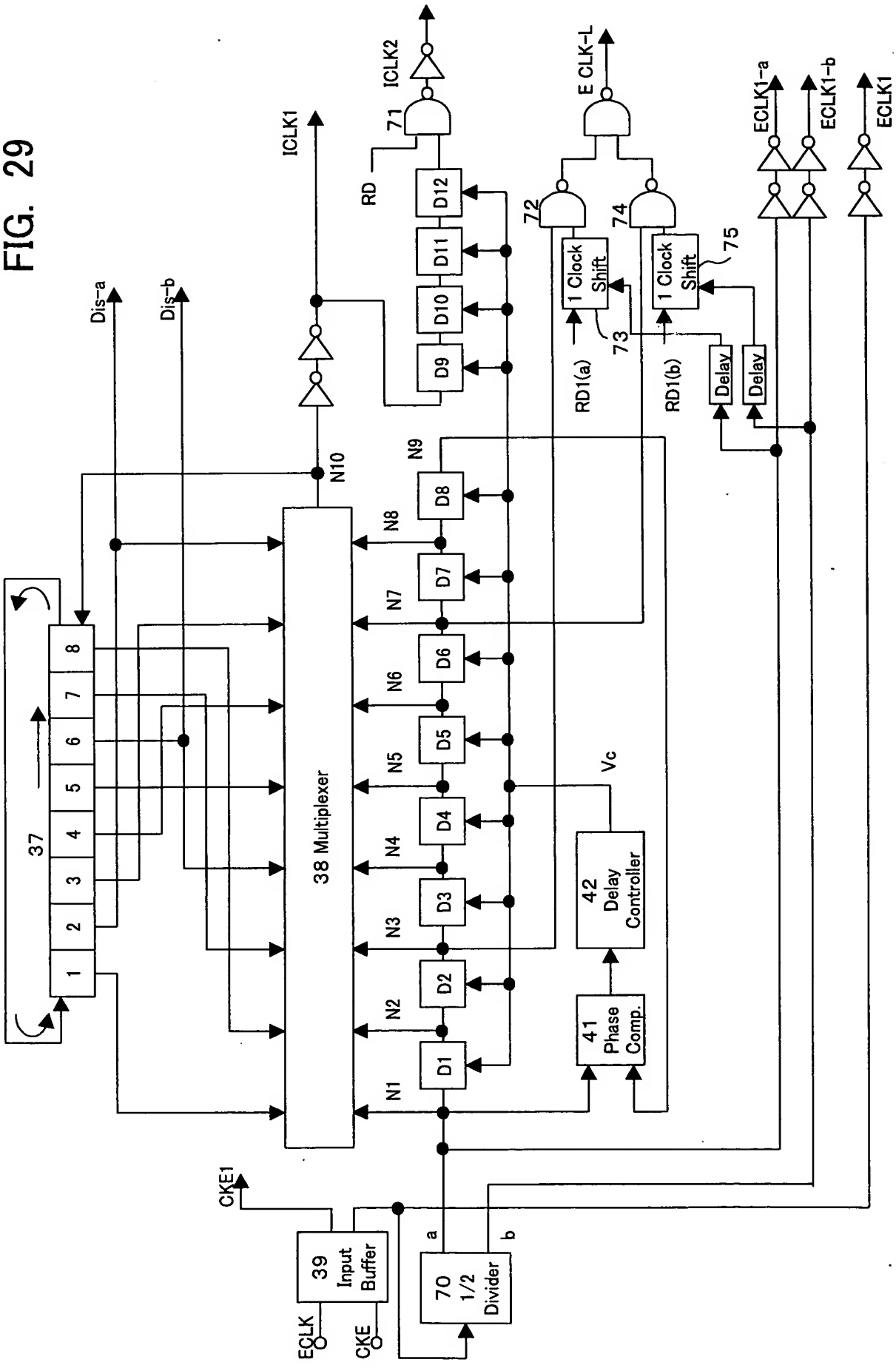

ICLK2
ICLK1
E CLK-L
ECLK1-a
ECLK1-b
ECLK1
RD
71
72
74
75
73
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
N9
N10
N8
N7
N6
N5
N4
N3
N2
N1
Dis-a
Dis-b
1 Clock Shift
1 Clock Shift
RD1(a)
RD1(b)
Delay
Delay
37
1
2
3
4
5
6
7
8
38 Multiplexer
Vc
42 Delay Controller
41 Phase Comp.
CKE1
39 Input Buffer
70 1/2 Divider
a
b
ECLK
CKE

FIG. 30

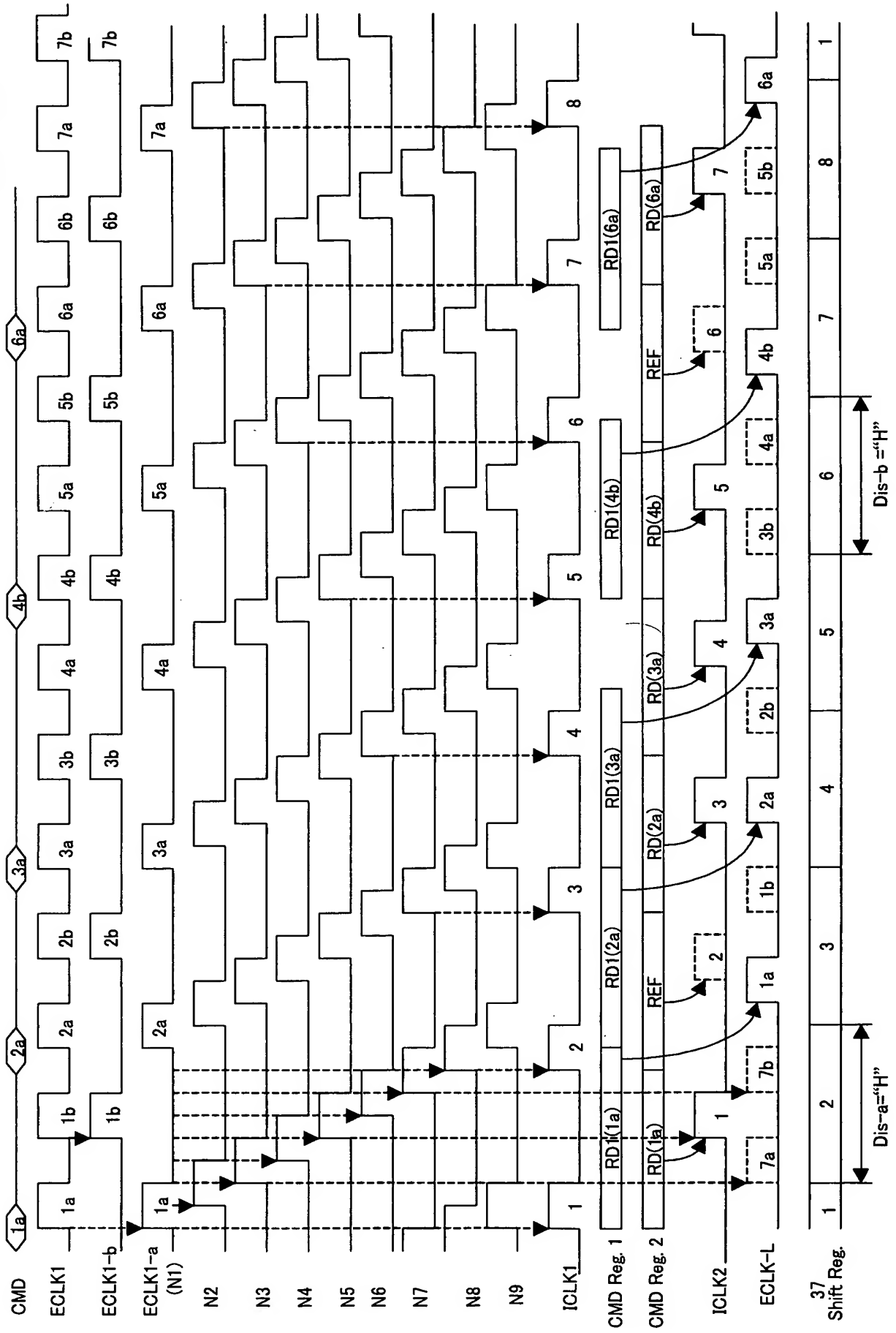

CMD
ECLK1
ECLK1-b
ECLK1-a
(N1)
N2
N3
N4
N5
N6
N7
N8
N9
ICLK1
CMD Reg. 1
CMD Reg. 2
ICLK2
ECLK-L
37
Shift Reg.
RD1(1a)
RD1(2a)
RD1(3a)
RD1(4b)
RD1(6a)
RD(1a)
RD(2a)
RD(3a)
RD(4b)
RD(6a)
REF
Dis-a="H"
Dis-b ="H"

FIG. 31

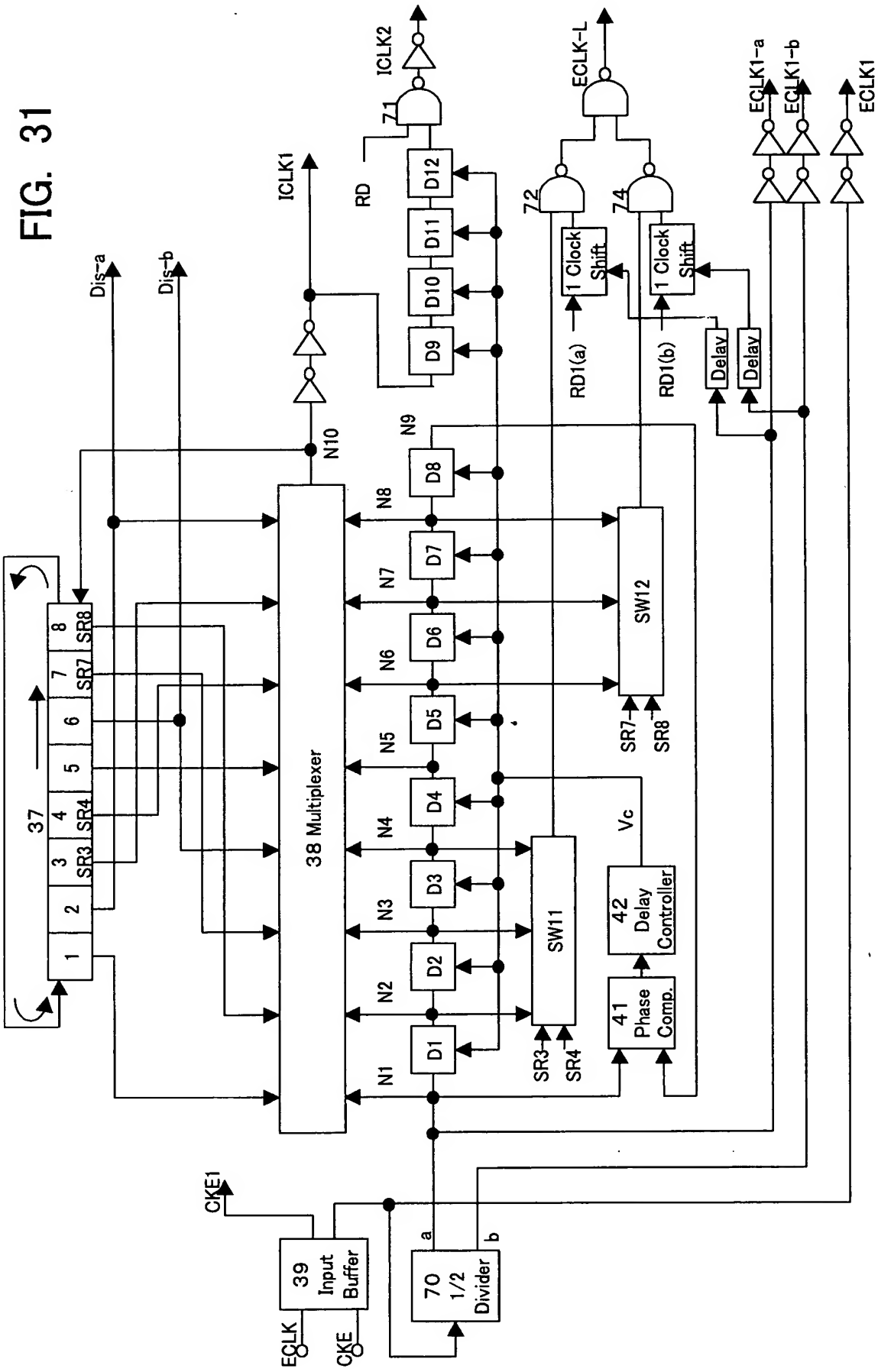

ICLK2
Z1
RD
ICLK1
ECLK-L
Z2
Z4
ECLK1-a
ECLK1-b
ECLK1
Dis-a
Dis-b
D12
D11
D10
D9
1 Clock Shift
1 Clock Shift
RD1(a)
RD1(b)
Delay
Delay
N10
N9
N8
N7
N6
N5
N4
N3
N2
N1
D8
D7
D6
D5
D4
D3
D2
D1
SW12
SW11
SR7
SR8
SR3
SR4
Vc
42 Delay Controller
41 Phase Comp.
37
1
2
3 SR3
4 SR4
5
6
7 SR7
8 SR8
38 Multiplexer
CKE1
39 Input Buffer
70 1/2 Divider
a
b
ECLK
CKE

FIG. 32

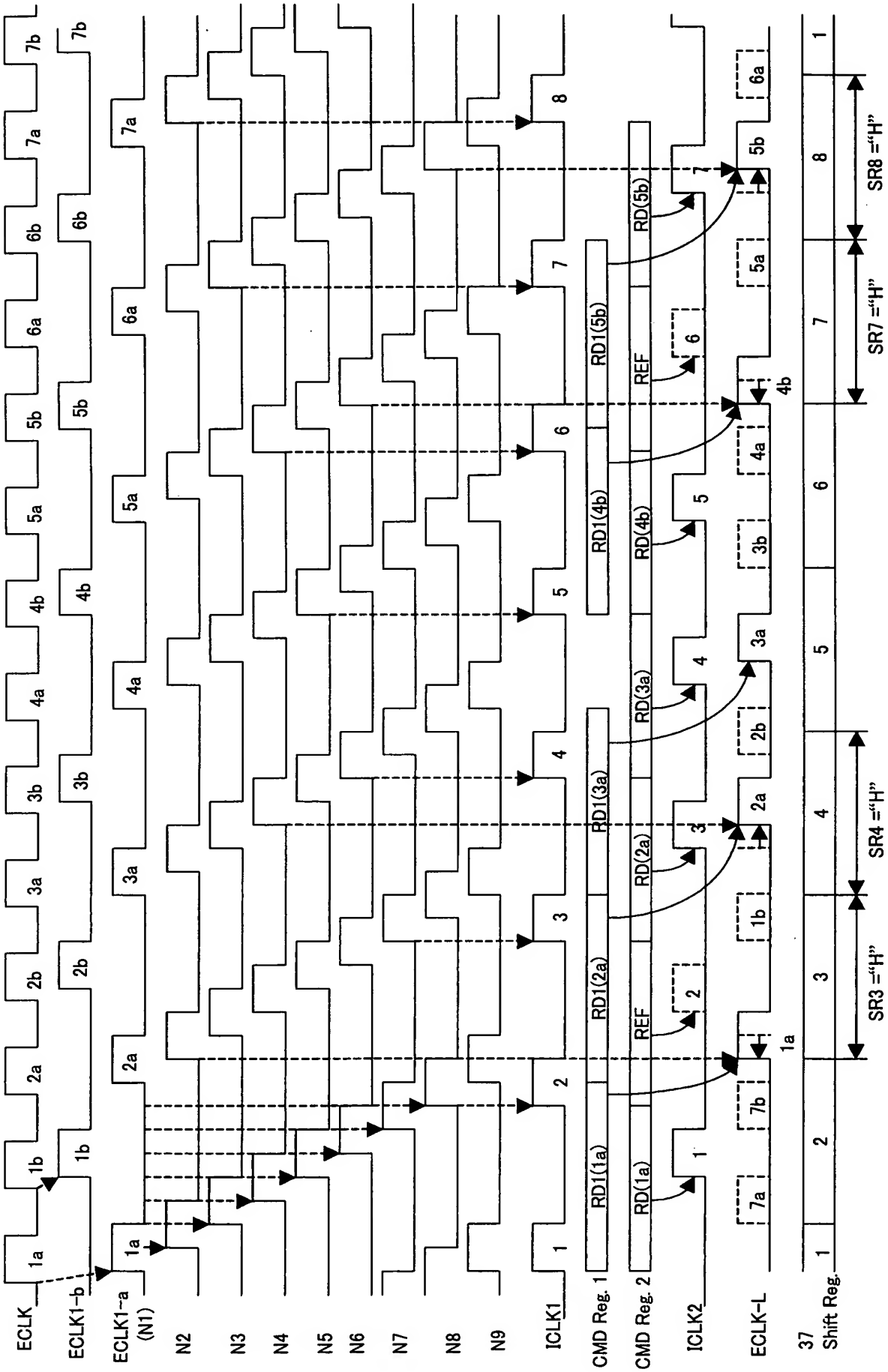
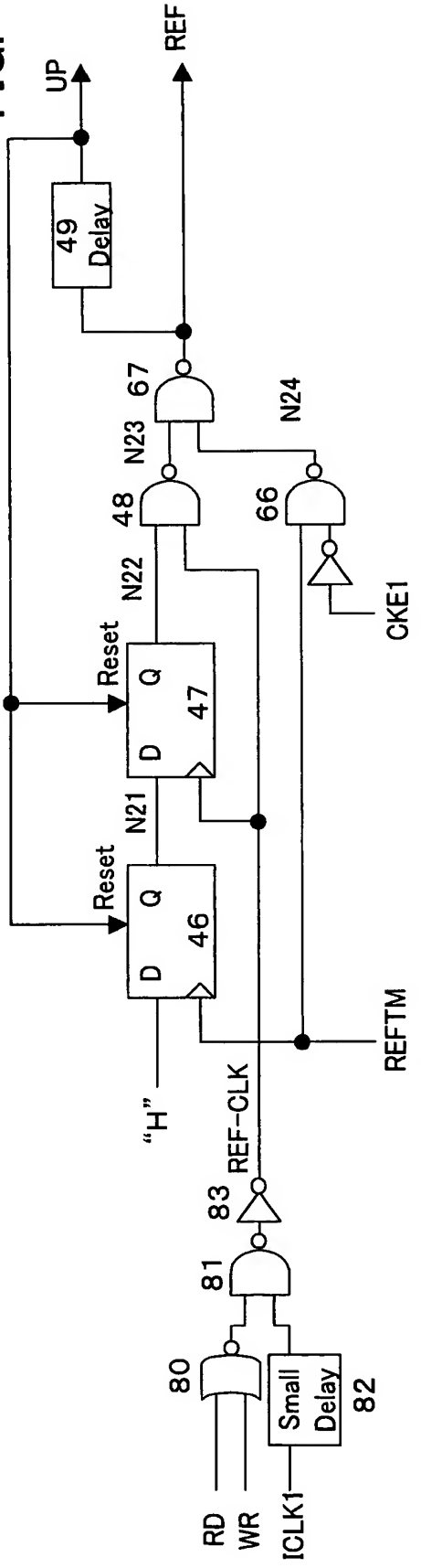

ECLK
ECLK1-b
ECLK1-a (N1)
N2
N3
N4
N5
N6
N7
N8
N9
ICLK1
CMD Reg. 1
CMD Reg. 2
ICLK2
ECLK-L
37 Shift Reg.
RD1(1a)
RD1(2a)
RD1(3a)
RD1(4b)
RD1(5b)
RD(1a)
RD(2a)
RD(3a)
RD(4b)
RD(5b)
REF
SR3 ="H"
SR4 ="H"
SR7 ="H"
SR8 ="H"

FIG. 33


UP
REF
49
Delay
67
N23
N24
48
66
N22
CKE1
Reset
Q
D
47
N21
Reset
Q
D
46
"H"
REFTM
REF-CLK
83
81
80
Small
Delay
82
RD
WR
ICLK1

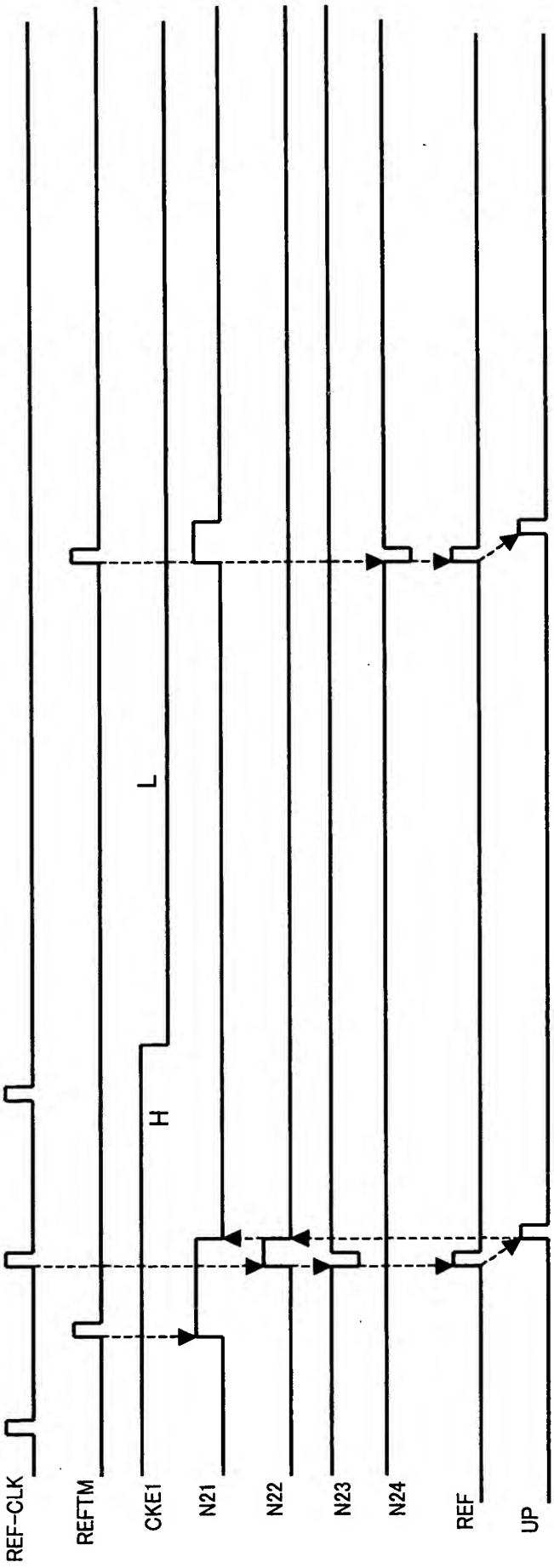

L
H
REF-CLK
REFTM
CKE1
N21
N22
N23
N24
REF
UP

FIG. 34

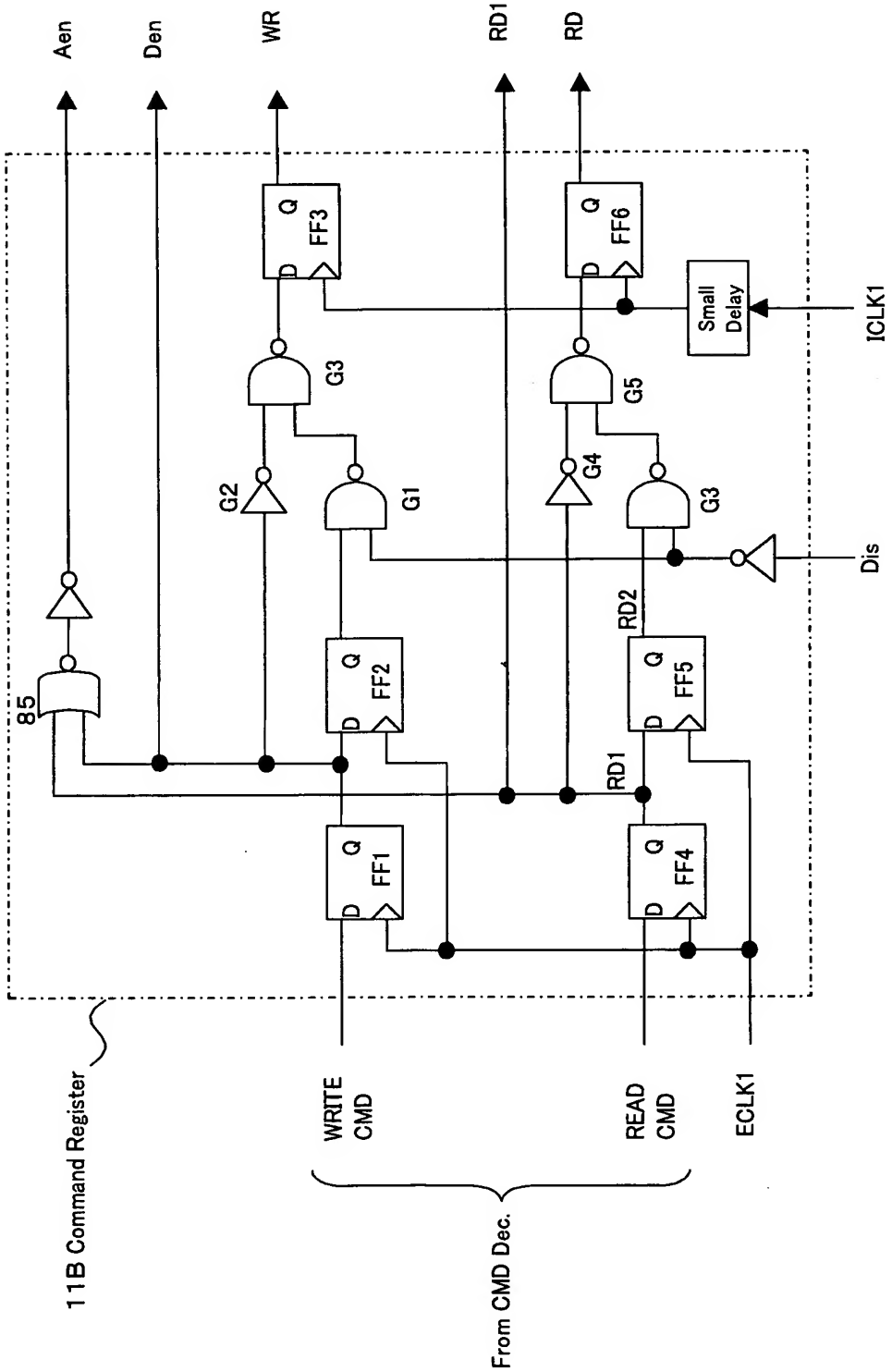

Aen
Den
WR
RD1
RD
FF3
FF6
Small Delay
ICLK1
G3
G5
G2
G1
G4
G3
Dis
RD2
85
FF2
FF5
RD1
FF1
FF4
11B Command Register
WRITE CMD
READ CMD
ECLK1
From CMD Dec.

FIG. 35

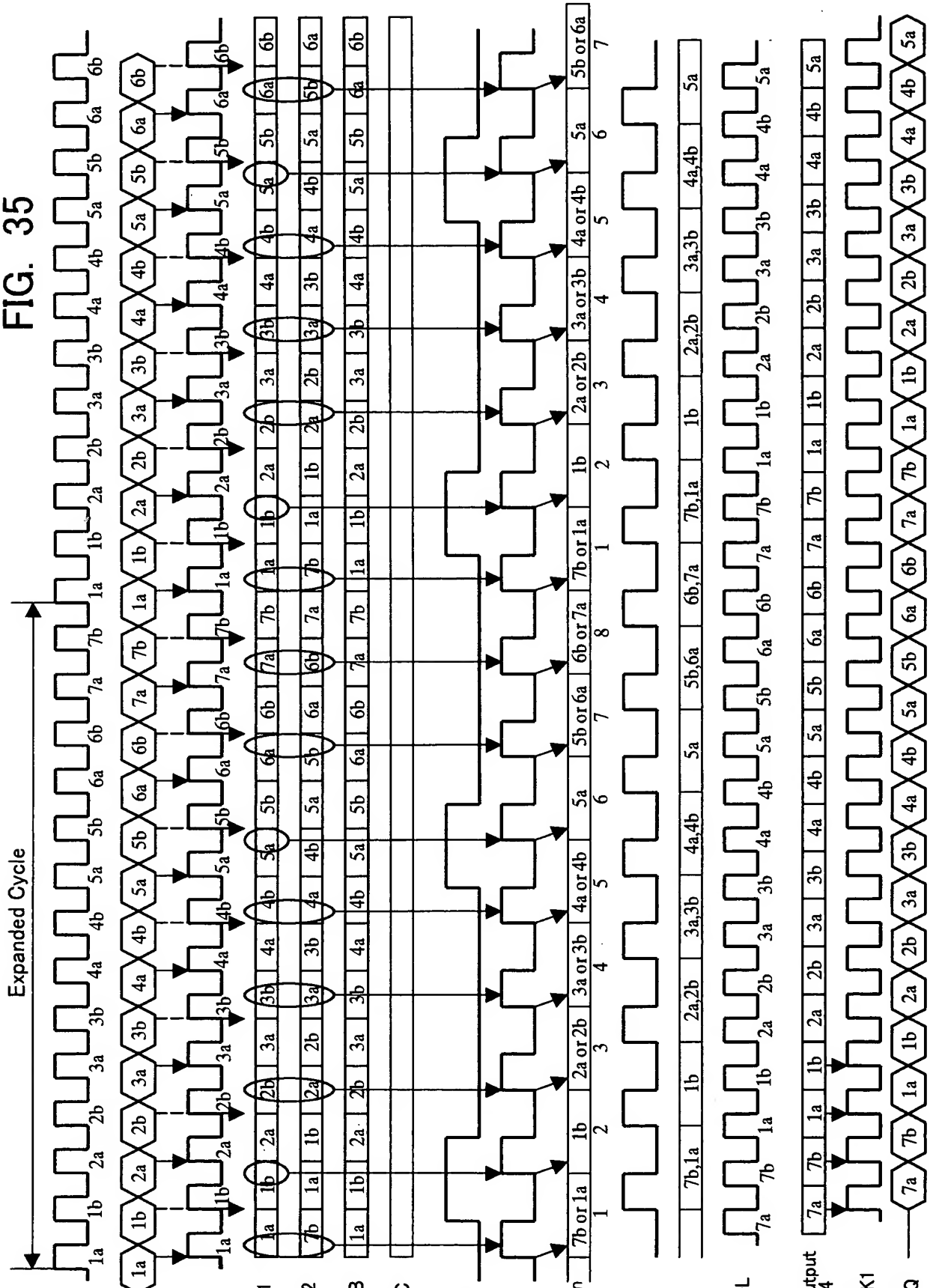

Expanded Cycle
ECLK
CMD
ECLK1
RD1
RD2
11B
12B
12C
Dis
ICLK1
Internal Operation Cycle
ICLK2
DB2
ECLK-L
Data Output Reg. 134
ECLK1
DQ

FIG. 36

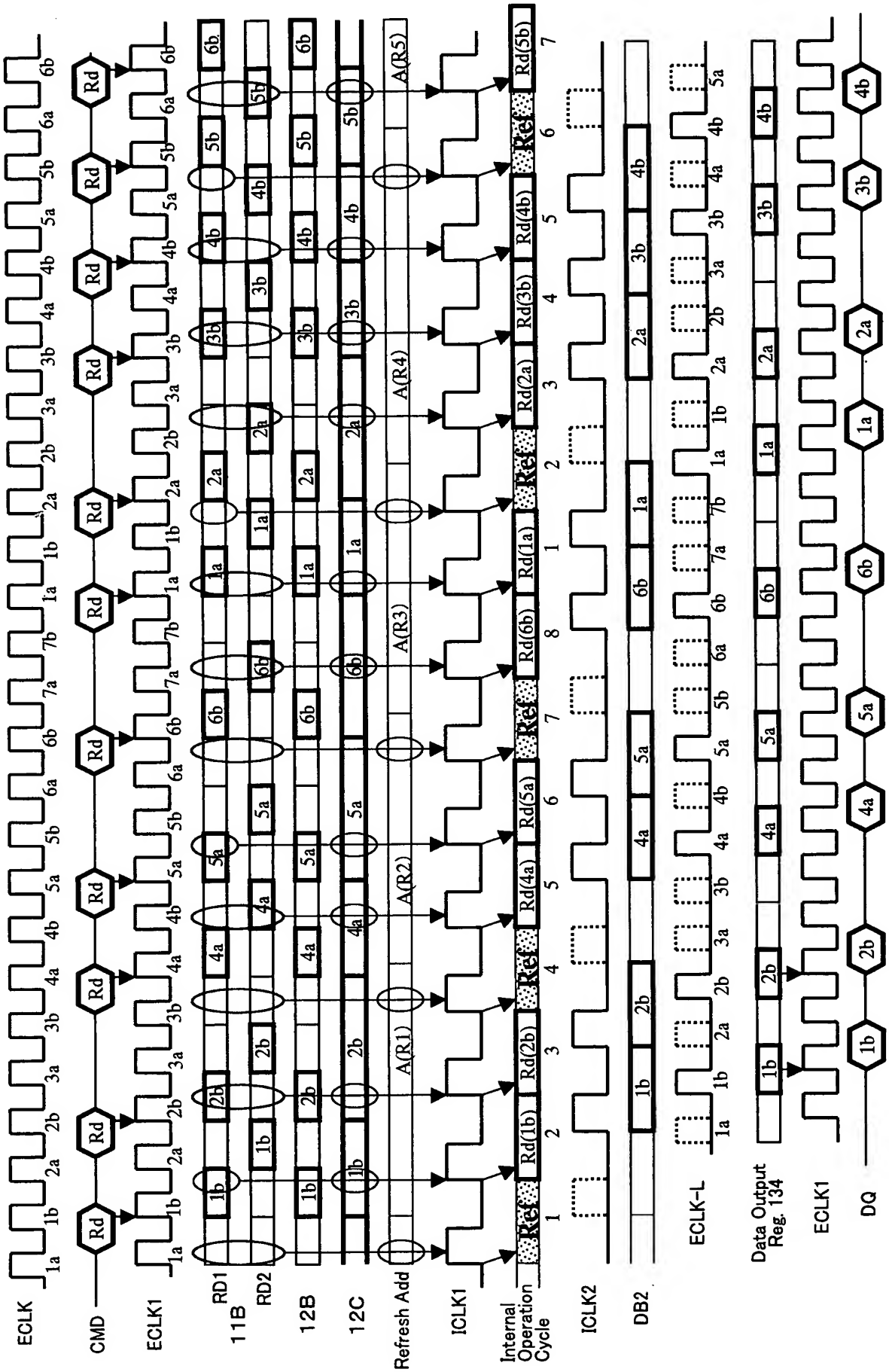

ECLK
CMD
ECLK1
RD1
11B
RD2
12B
12C
Refresh Add
ICLK1
Internal Operation Cycle
ICLK2
DB2
ECLK-L
Data Output Reg. 134
ECLK1
DQ
Rd
Ref
A(R1)
A(R2)
A(R3)
A(R4)
A(R5)
Rd(1b)
Rd(2b)
Rd(4a)
Rd(5a)
Rd(6b)
Rd(1a)
Rd(2a)
Rd(3b)
Rd(4b)
Rd(5b)

FIG. 37

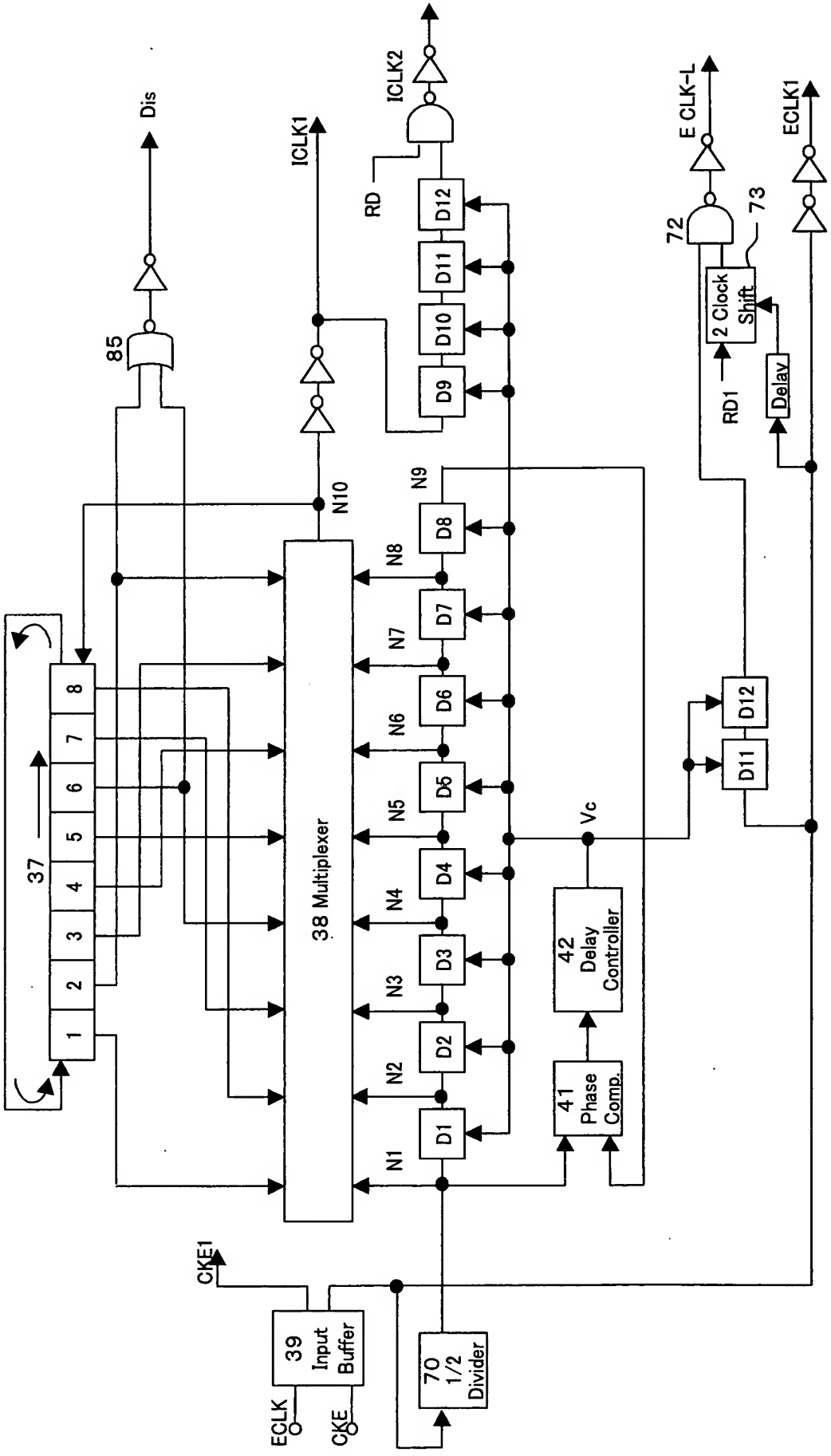

Dis
ICLK1
ICLK2
RD
E CLK-L
ECLK1
72
73
85
2 Clock Shift
RD1
Delay
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
N9
N10
N8
N7
N6
N5
N4
N3
N2
N1
Vc
37
1
2
3
4
5
6
7
8
38 Multiplexer
42 Delay Controller
41 Phase Comp.
CKE1
39 Input Buffer
70 1/2 Divider
ECLK
CKE

FIG. 38

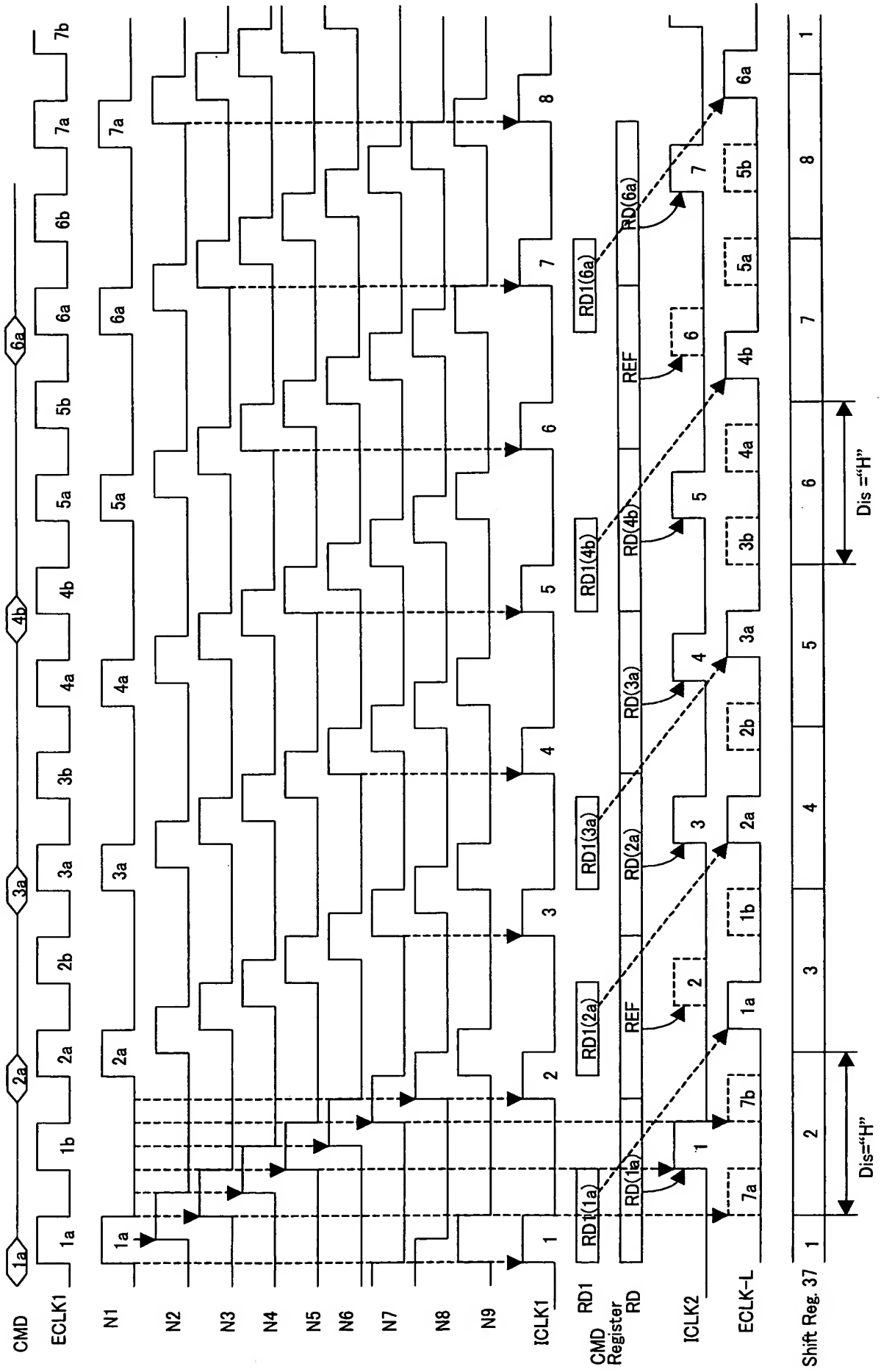

CMD
ECLK1
N1
N2
N3
N4
N5
N6
N7
N8
N9
ICLK1
RD1
CMD Register
RD
ICLK2
ECLK-L
Shift Reg. 37
RD1(1a)
RD1(2a)
RD1(3a)
RD1(4b)
RD1(6a)
RD(1a)
RD(2a)
RD(3a)
RD(4b)
RD(6a)
REF
Dis="H"
Dis ="H"

FIG. 39
Fifth Embodiment

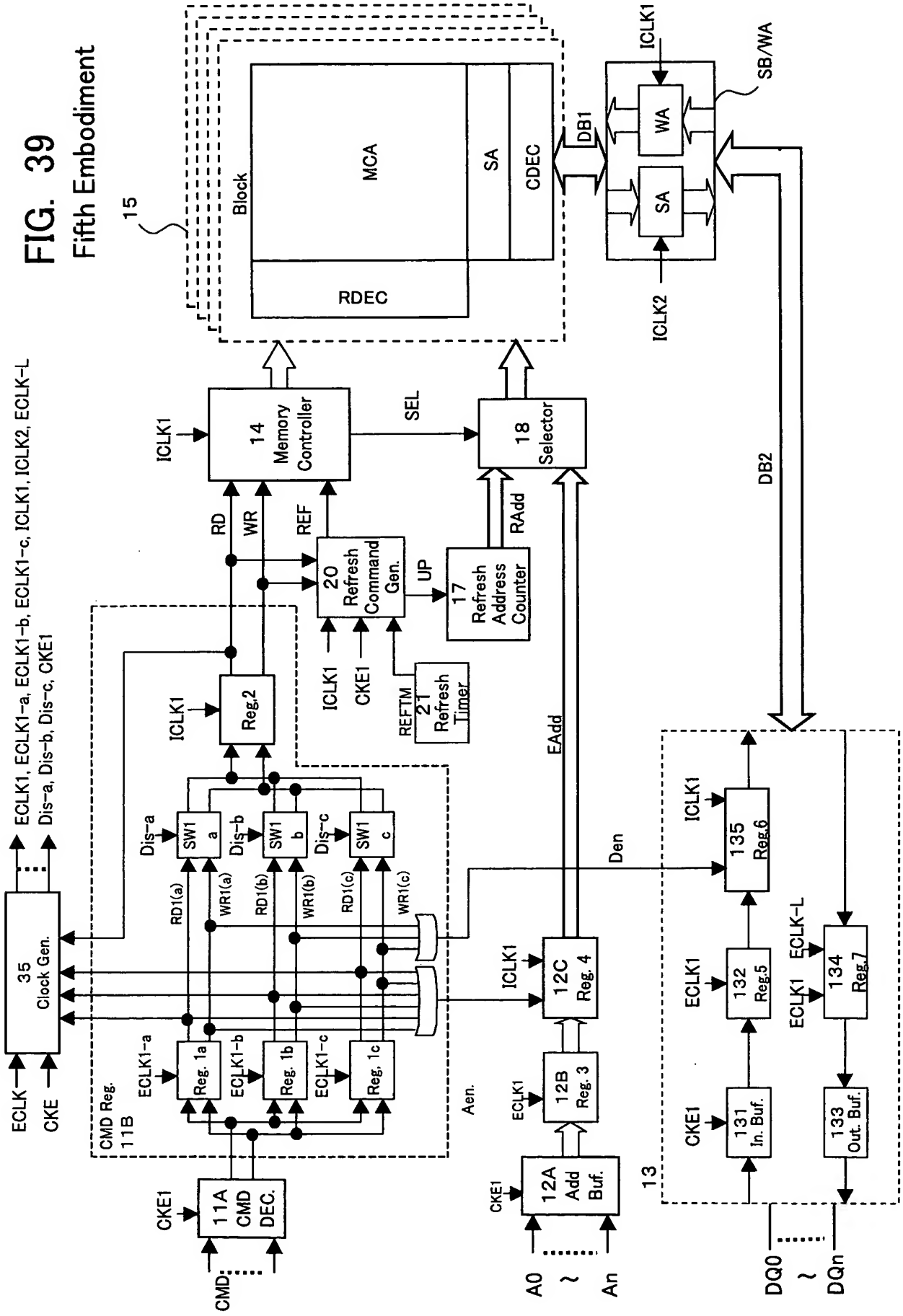


FIG. 40

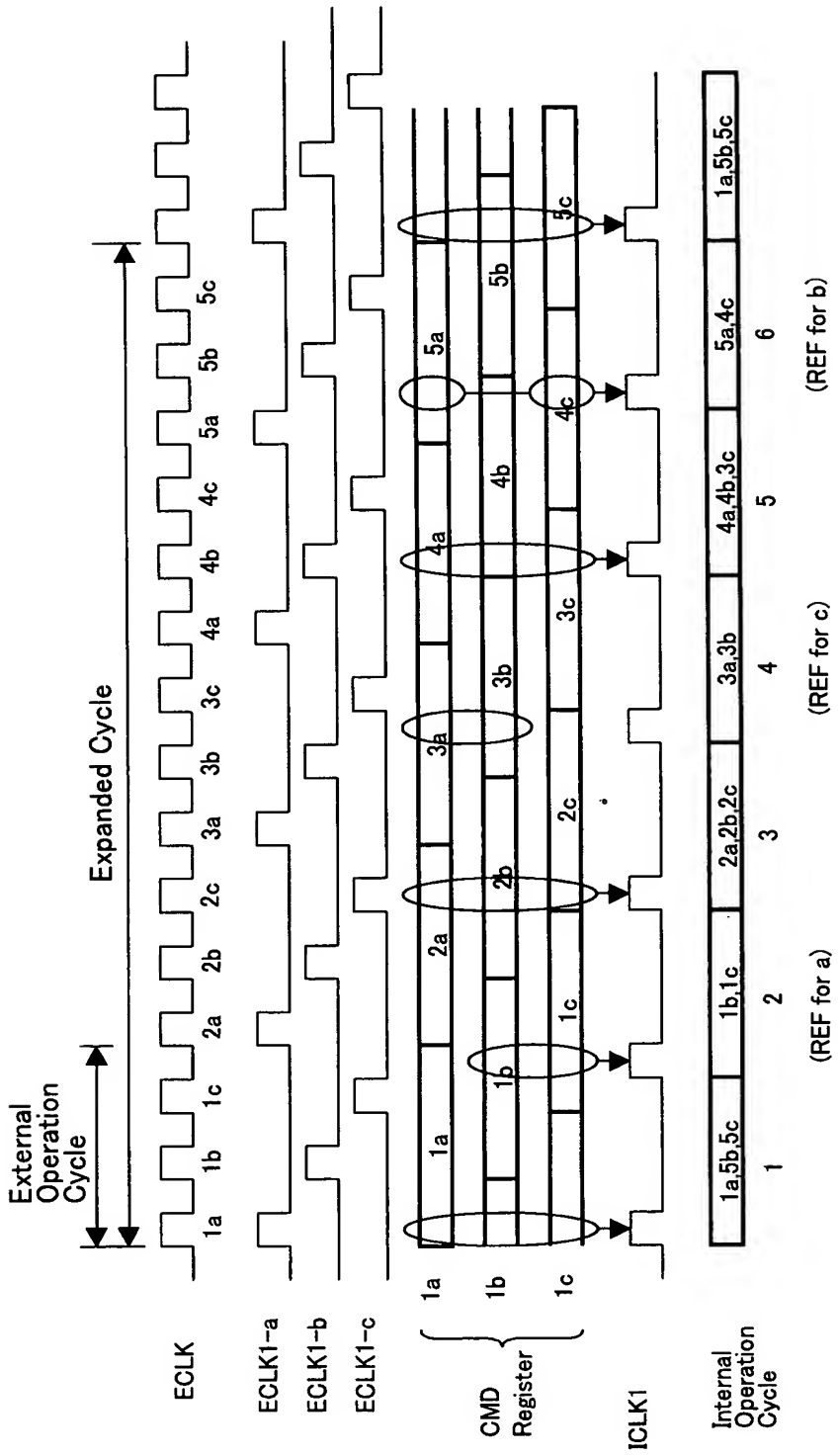

External Operation Cycle
Expanded Cycle
ECLK
ECLK1-a
ECLK1-b
ECLK1-c
CMD Register
ICLK1
Internal Operation Cycle
1a 1b 1c 2a 2b 2c 3a 3b 3c 4a 4b 4c 5a 5b 5c
1a,5b,5c
1b,1c
2a,2b,2c
3a,3b
4a,4b,3c
5a,4c
1 2 3 4 5 6
(REF for a)
(REF for c)
(REF for b)
External Operation Cycle = 3ECLK

FIG. 41

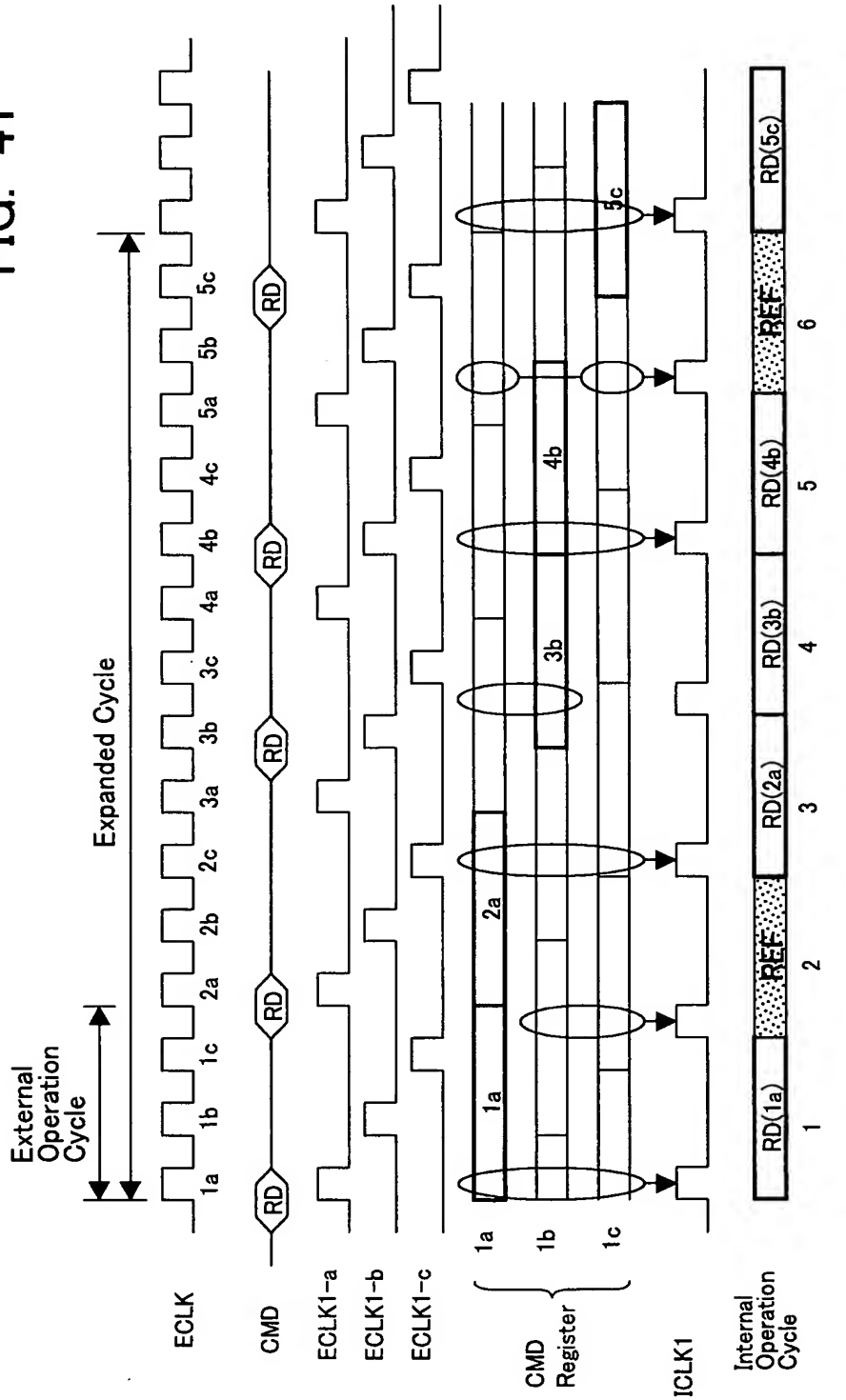

External Operation Cycle
Expanded Cycle
ECLK
CMD
ECLK1-a
ECLK1-b
ECLK1-c
CMD Register
ICLK1
Internal Operation Cycle
RD
REF
RD(1a)
RD(2a)
RD(3b)
RD(4b)
RD(5c)

FIG. 42

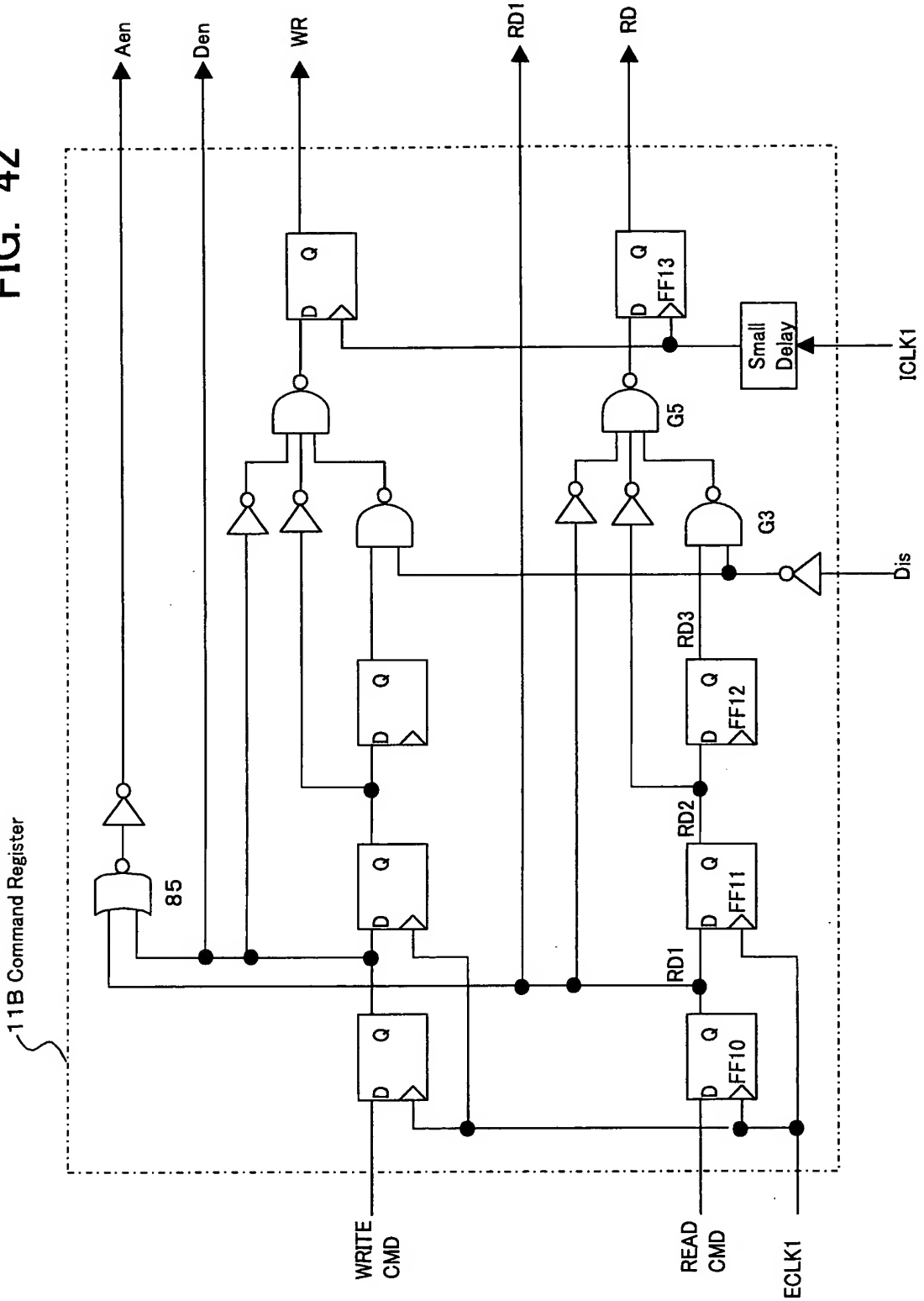
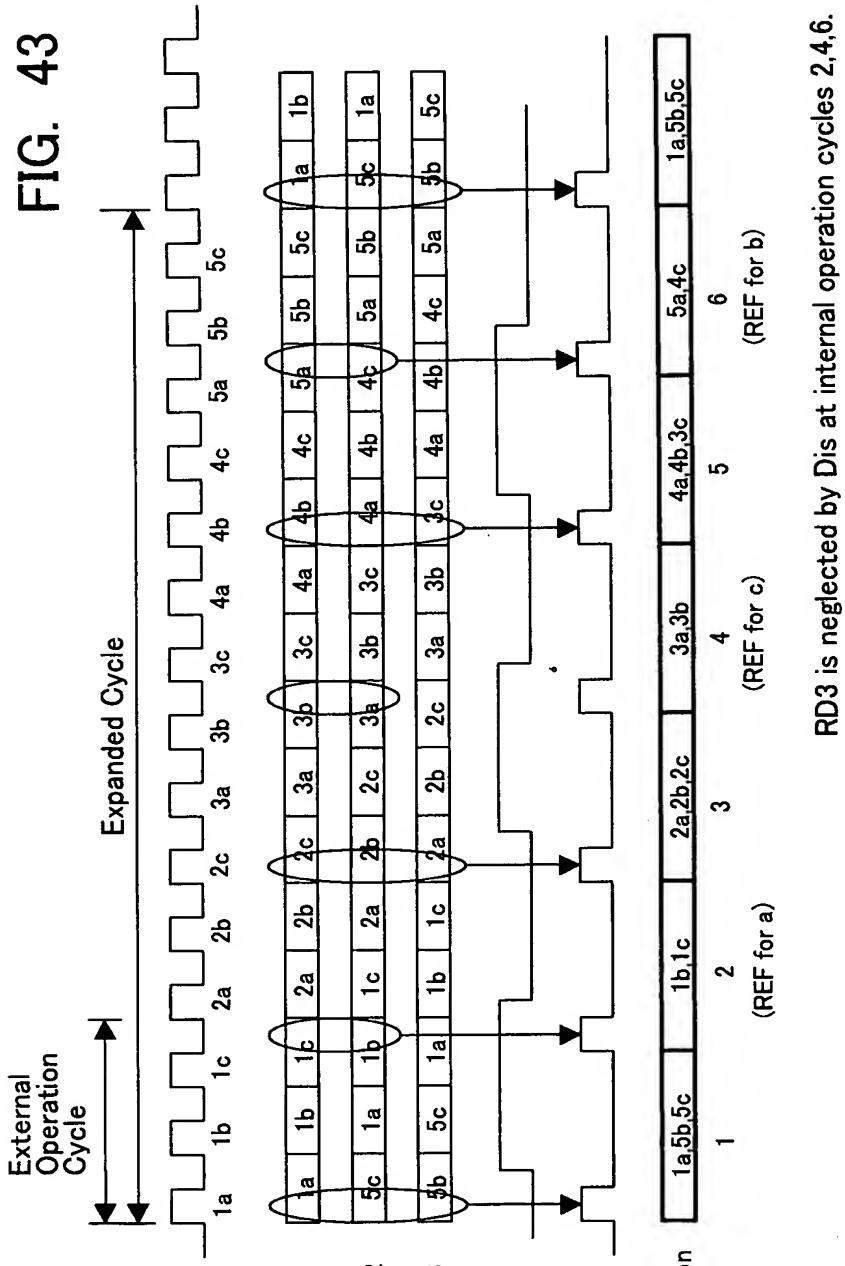

Aen
Den
WR
RD1
RD
11B Command Register
85
Q
D
FF13
Small Delay
ICLK1
G5
G3
Dis
RD3
FF12
RD2
FF11
RD1
FF10
WRITE CMD
READ CMD
ECLK1

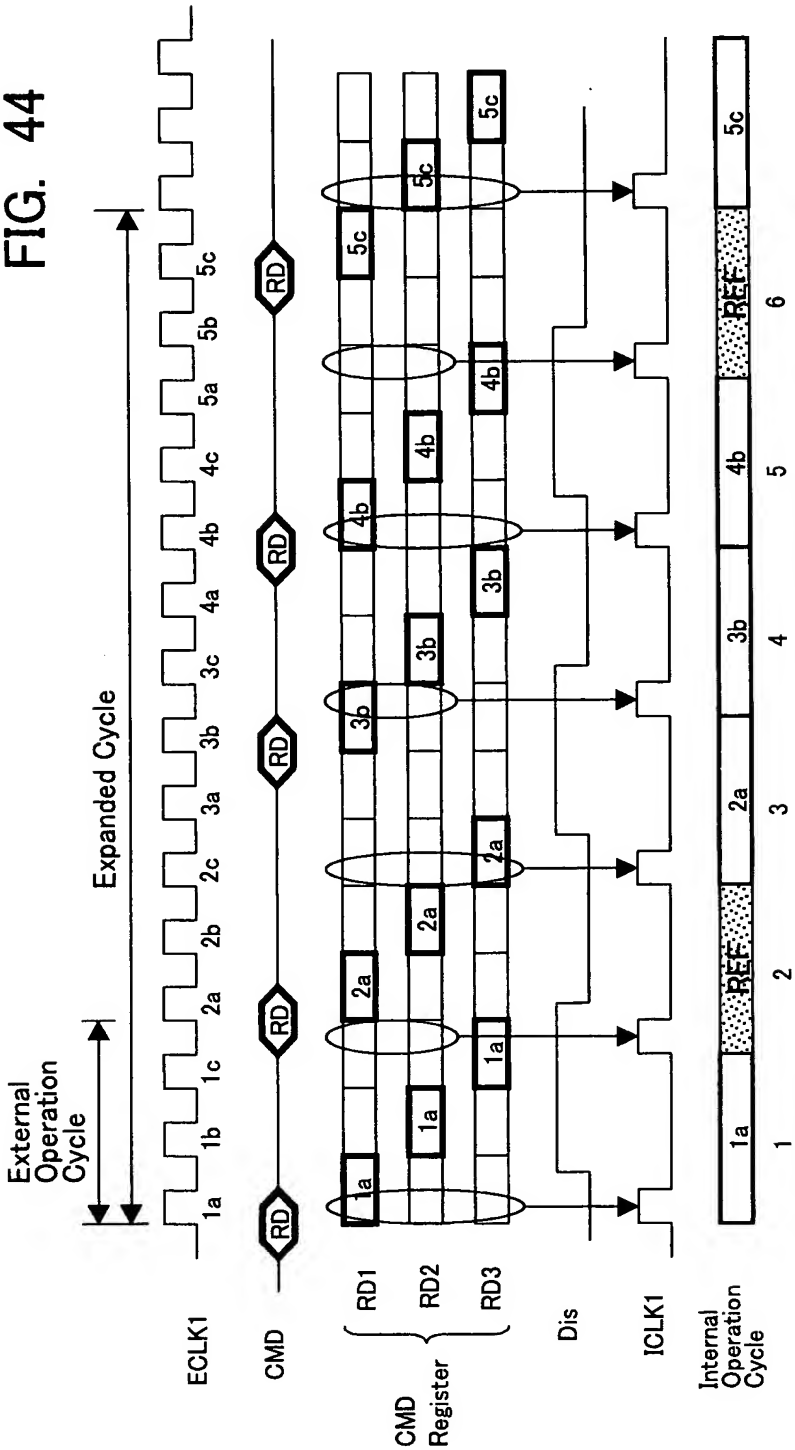
FIG. 43



RD3 is neglected by Dis at internal operation cycles 2,4,6.

External Operation Cycle = 3ECLK

FIG. 44



RD3 is neglected by Dis at internal operation cycles 2,4,6.

FIG. 45

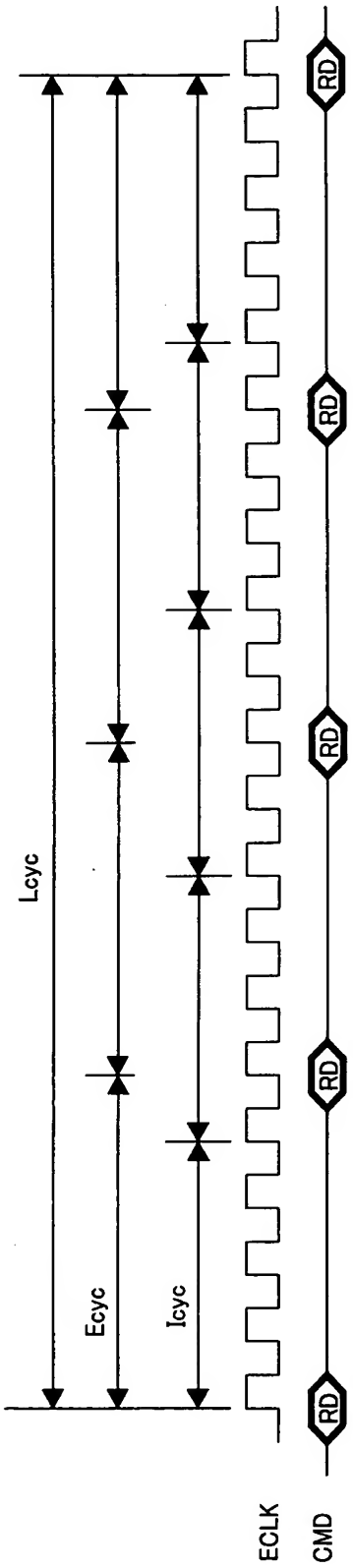


FIG. 46

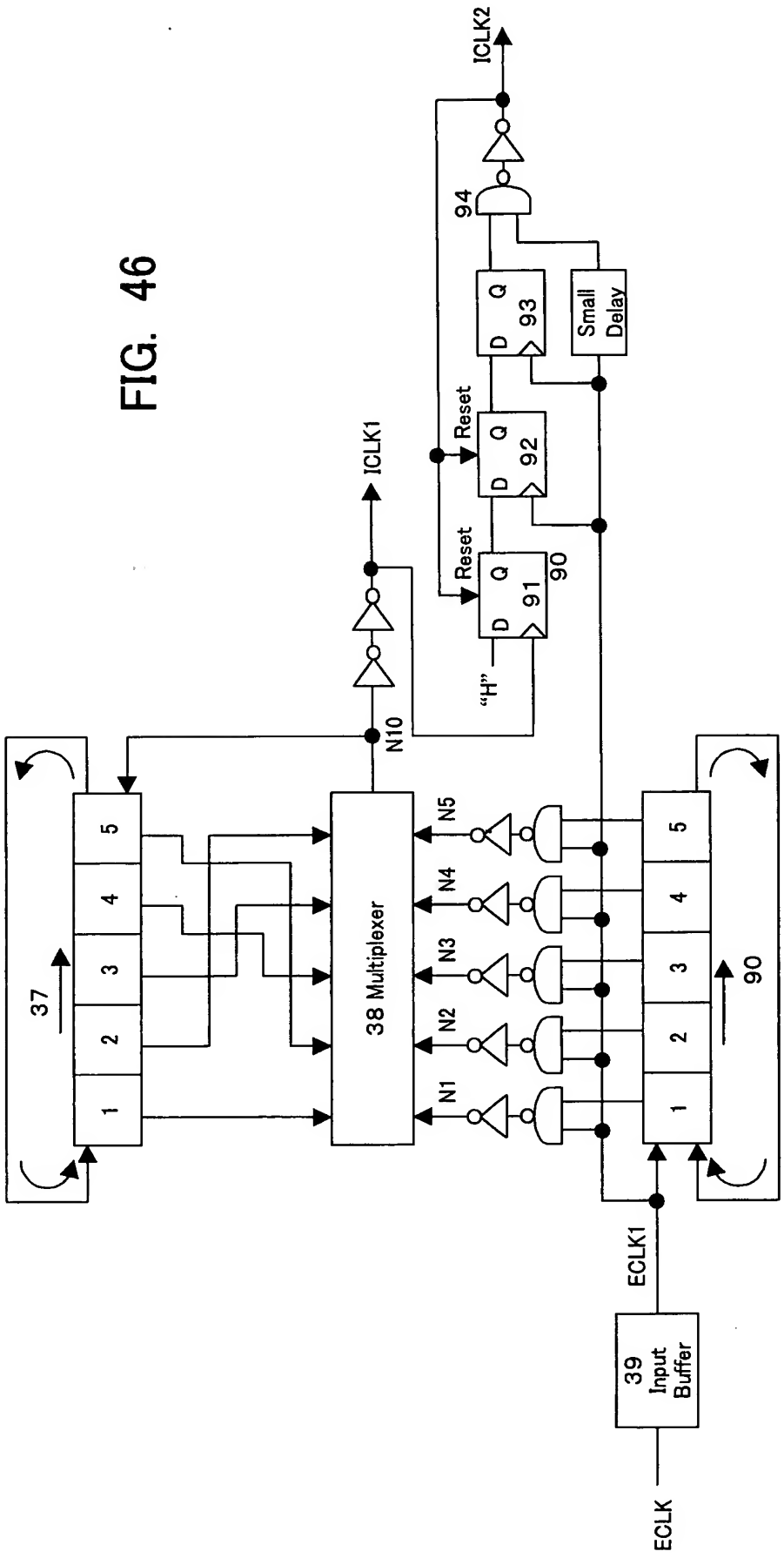

ICLK2
94
Q
D
93
Small Delay
Reset
Q
D
92
ICLK1
Reset
Q
D
91
90
"H"
N10
N5
N4
N3
N2
N1
38 Multiplexer
37
1
2
3
4
5
90
ECLK1
39 Input Buffer
ECLK

FIG. 47

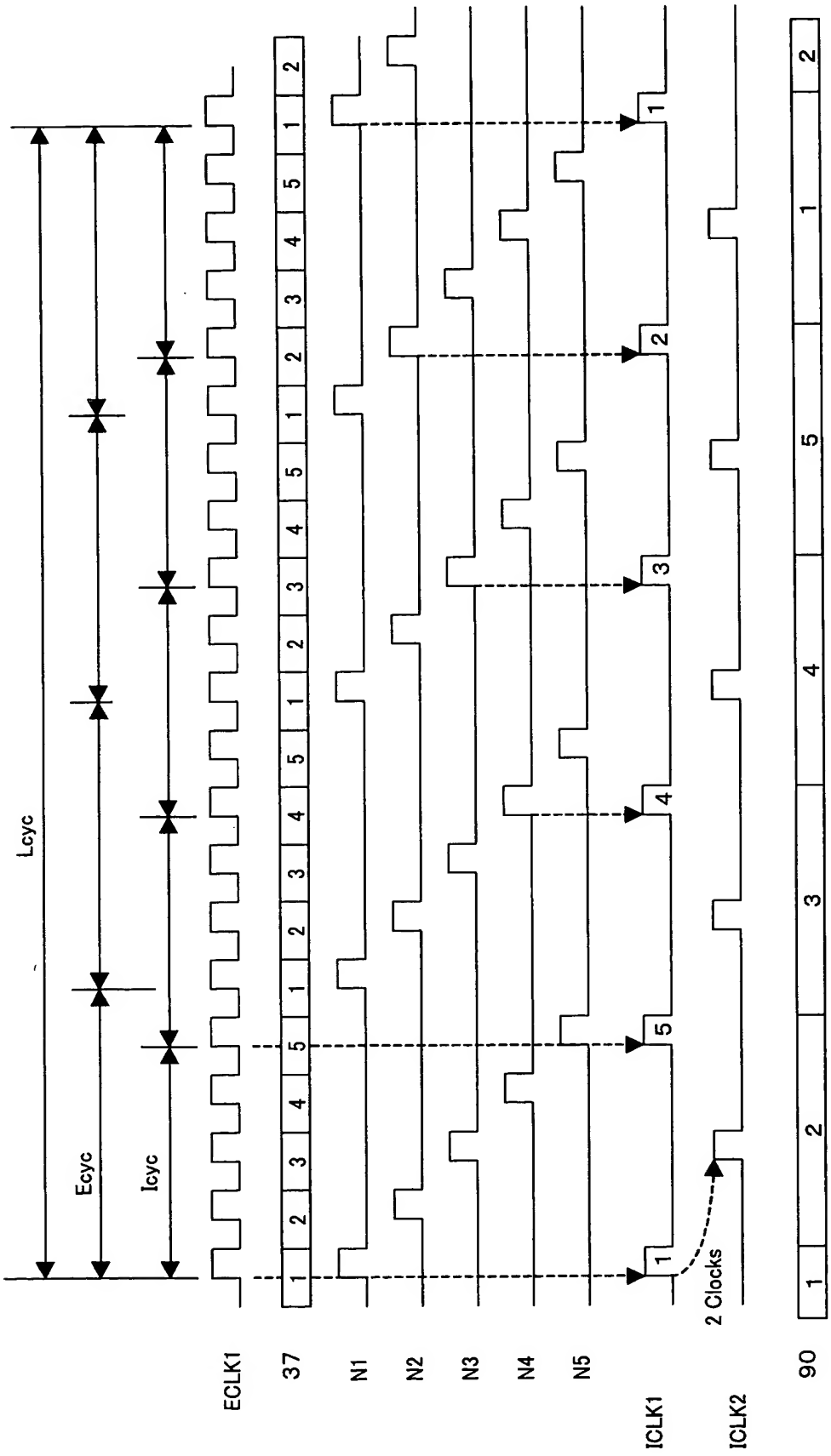


FIG. 48

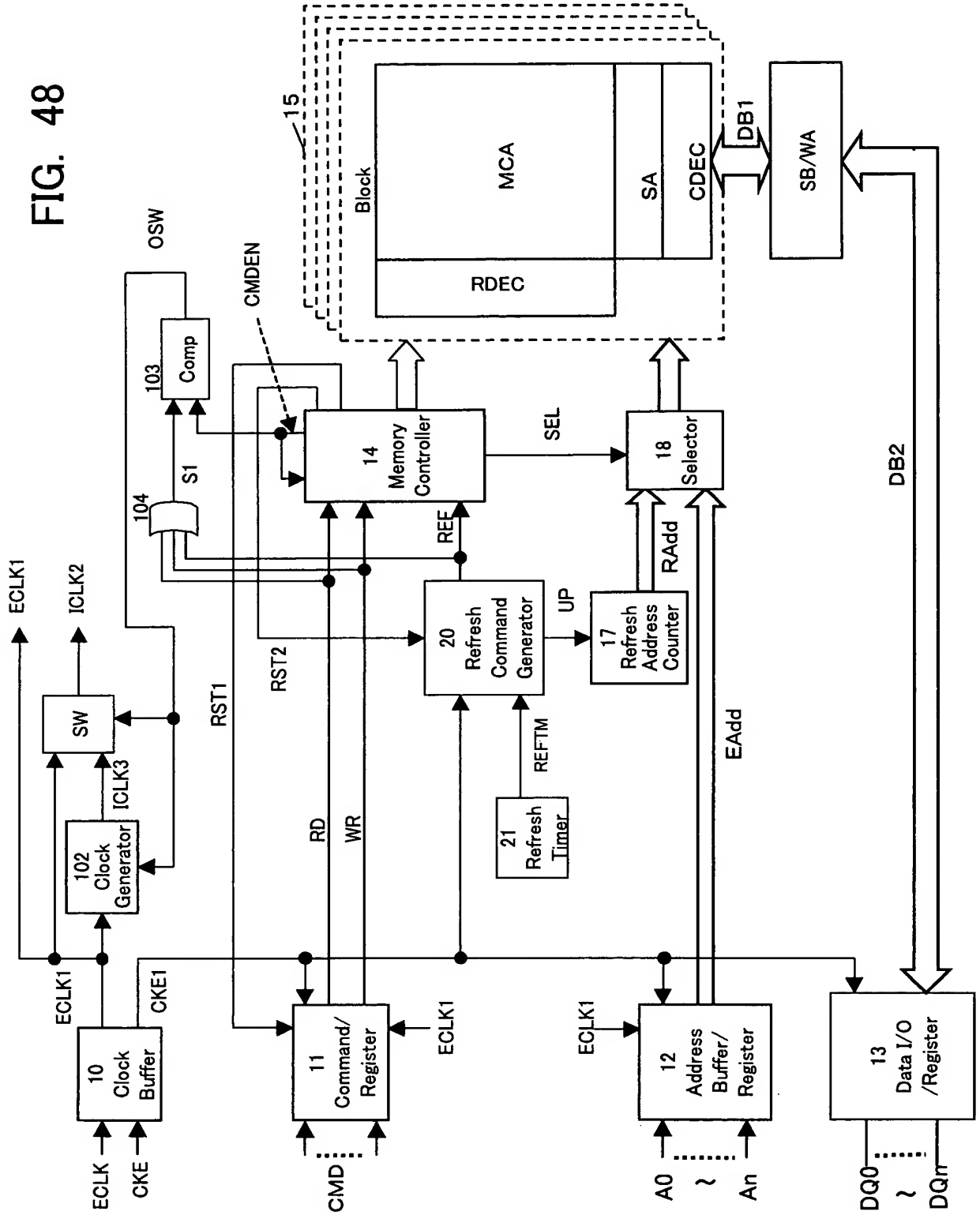

15
Block
MCA
SA
CDEC
RDEC
DB1
SB/WA
DB2
OSW
CMDEN
103
Comp
104
S1
14
Memory
Controller
SEL
18
Selector
REE
RAdd
ECLK1
ICLK2
20
Refresh
Command
Generator
UP
17
Refresh
Address
Counter
SW
RST1
RST2
ICLK3
102
Clock
Generator
RD
WR
REFTM
21
Refresh
Timer
EAdd
ECLK1
CKE1
ECLK1
ECLK1
10
Clock
Buffer
11
Command/
Register
12
Address
Buffer/
Register
13
Data I/O
/Register
ECLK
CKE
CMD
A0
~
An
DQ0
~
DQm

FIG. 49

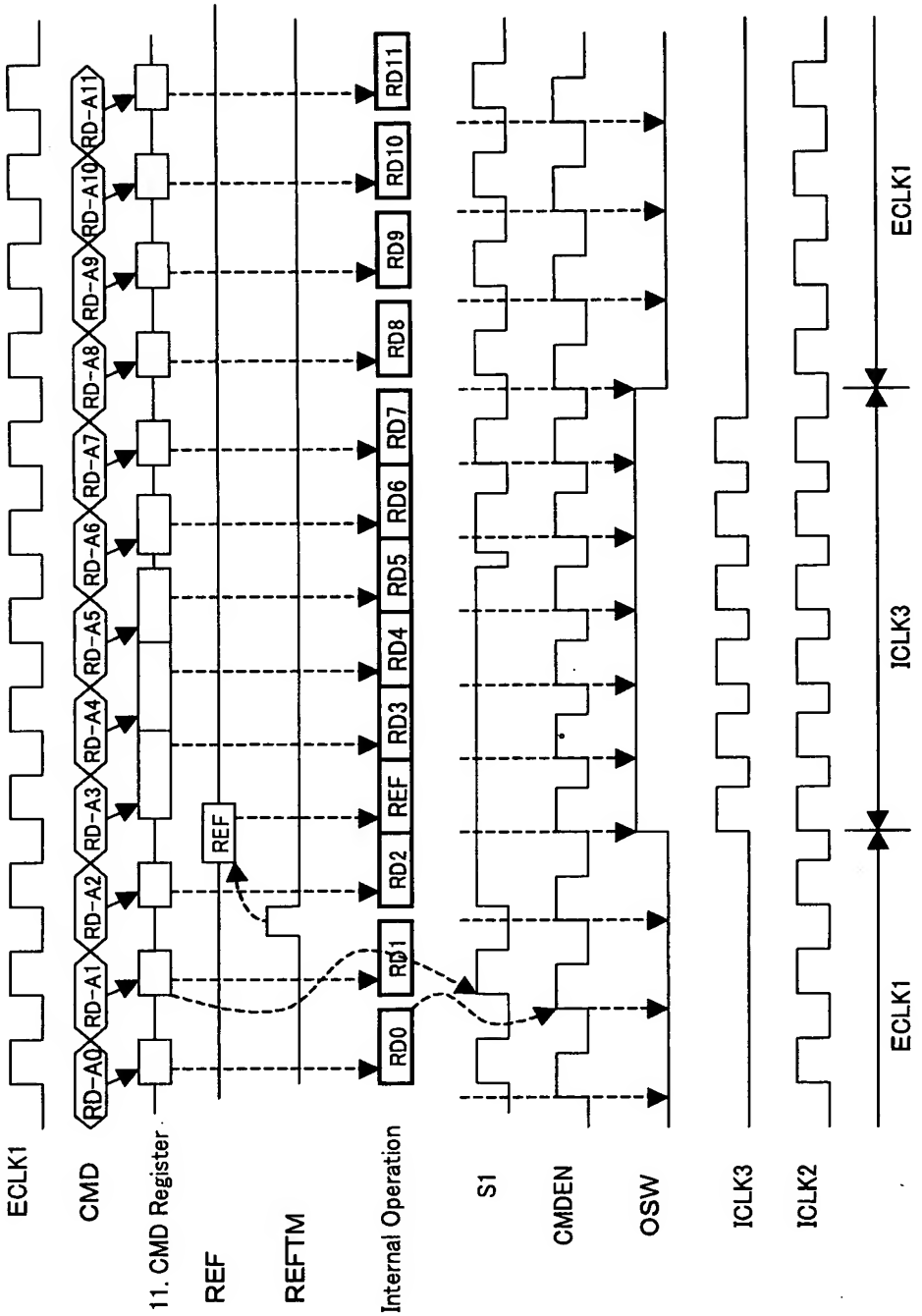
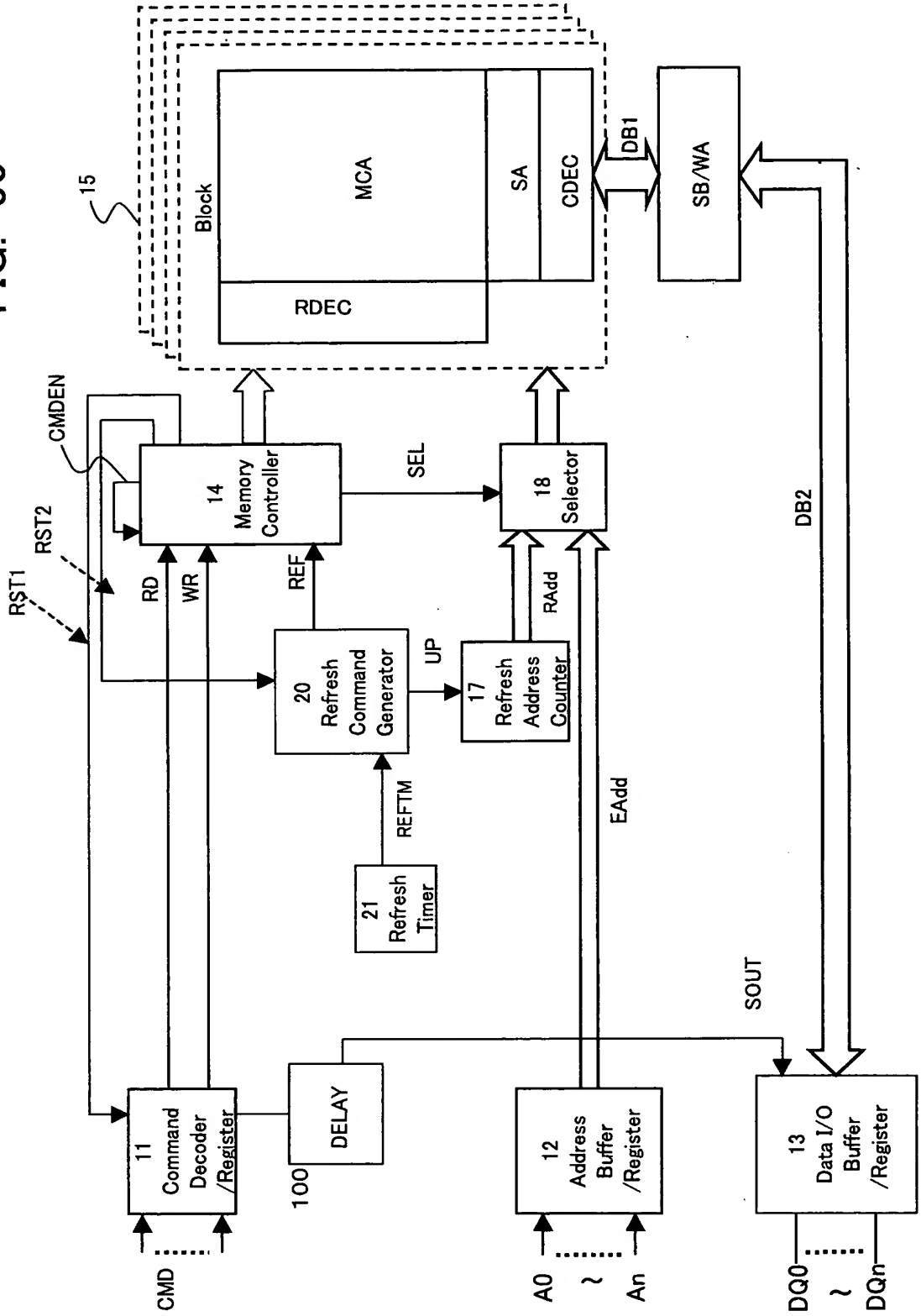

ECLK1
CMD
RD-A0
RD-A1
RD-A2
RD-A3
RD-A4
RD-A5
RD-A6
RD-A7
RD-A8
RD-A9
RD-A10
RD-A11
11. CMD Register
REF
REFTM
Internal Operation
RD0
RD1
RD2
REF
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
S1
CMDEN
OSW
ICLK3
ICLK2
ECLK1
ICLK3
ECLK1

FIG. 50


15
Block
MCA
SA
CDEC
RDEC
DB1
SB/WA
DB2
CMDEN
RST2
RST1
14 Memory Controller
SEL
18 Selector
RD
WR
REF
RAdd
20 Refresh Command Generator
UP
17 Refresh Address Counter
REFTM
21 Refresh Timer
EAdd
SOUT
11 Command Decoder /Register
DELAY
100
12 Address Buffer /Register
13 Data I/O Buffer /Register
CMD
A0
~
An
DQ0
~
DQn

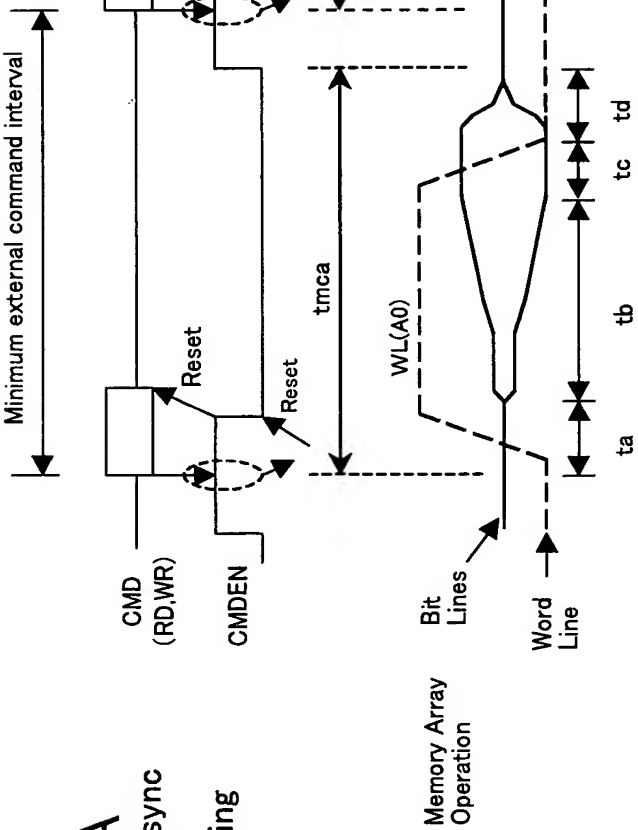


FIG. 51A
Operation in sync with external command timing

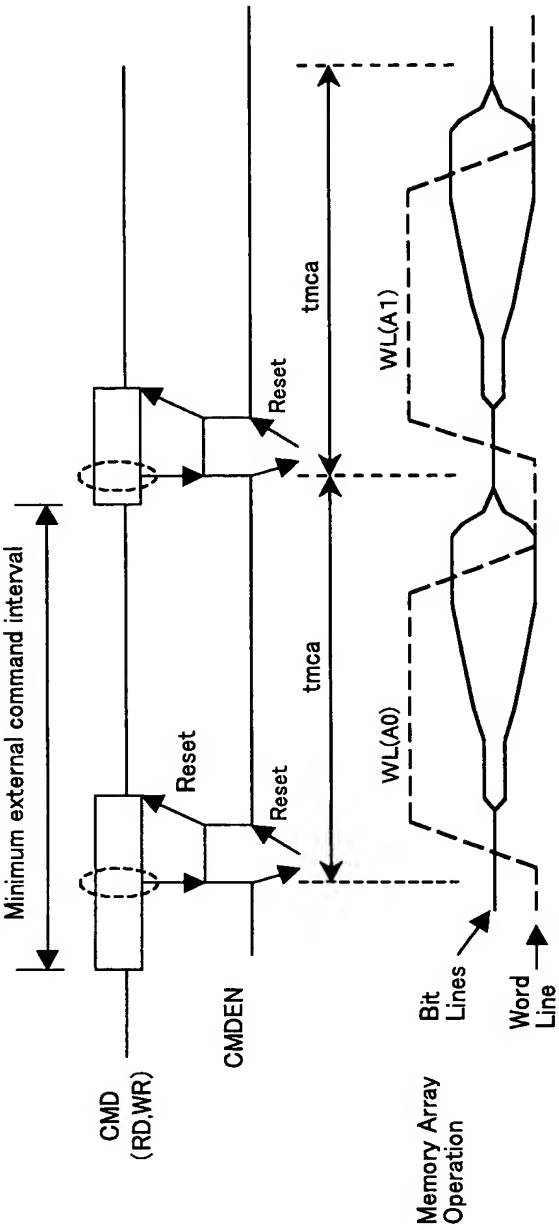


FIG. 51B
Operation asynchronous with external command timing

FIG. 52

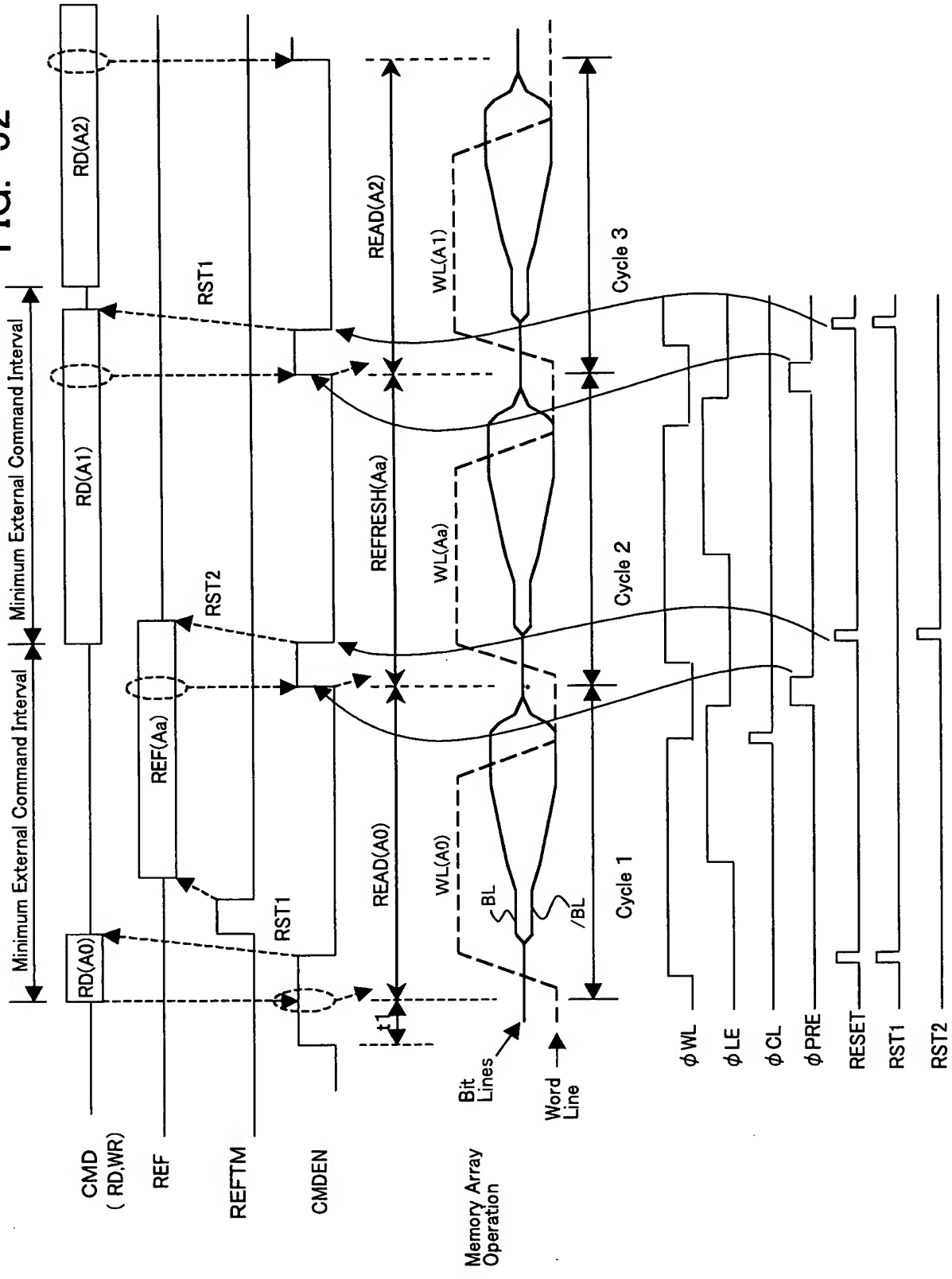
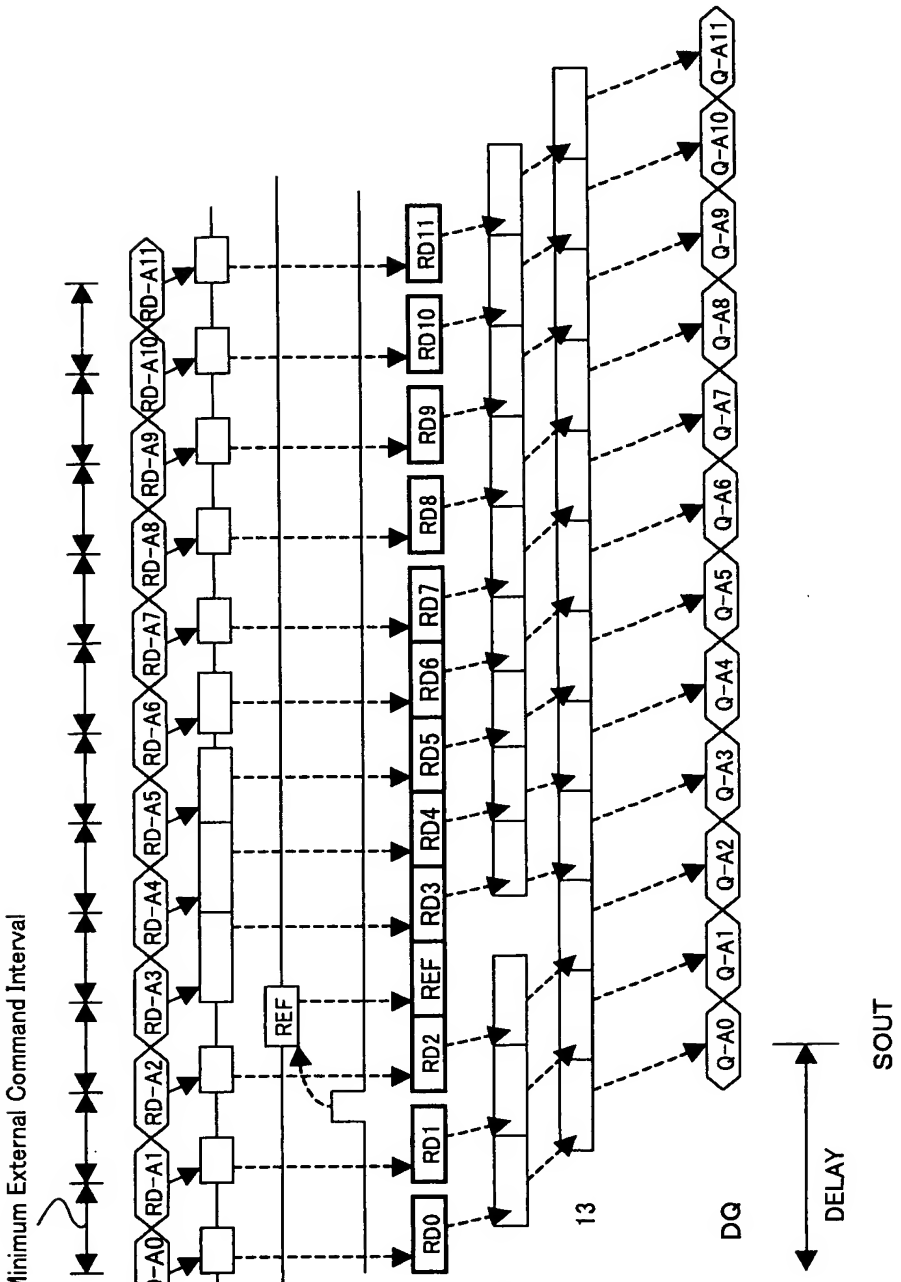

CMD (RD,WR)
REF
REFTM
CMDEN
Memory Array Operation
Bit Lines
Word Line
RD(A0)
RD(A1)
RD(A2)
REF(Aa)
RST1
RST2
READ(A0)
REFRESH(Aa)
READ(A2)
WL(A0)
WL(Aa)
WL(A1)
BL
/BL
t1
Minimum External Command Interval
Minimum External Command Interval
Cycle 1
Cycle 2
Cycle 3
φWL
φLE
φCL
φPRE
RESET
RST1
RST2

FIG. 53


Minimum External Command Interval
CMD
11
REF.
REFTM.
Internal Operation
DB
13
DQ
DELAY
SOUT
RD-A0
RD-A1
RD-A2
RD-A3
RD-A4
RD-A5
RD-A6
RD-A7
RD-A8
RD-A9
RD-A10
RD-A11
REF
RD0
RD1
RD2
REF
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
Q-A0
Q-A1
Q-A2
Q-A3
Q-A4
Q-A5
Q-A6
Q-A7
Q-A8
Q-A9
Q-A10
Q-A11